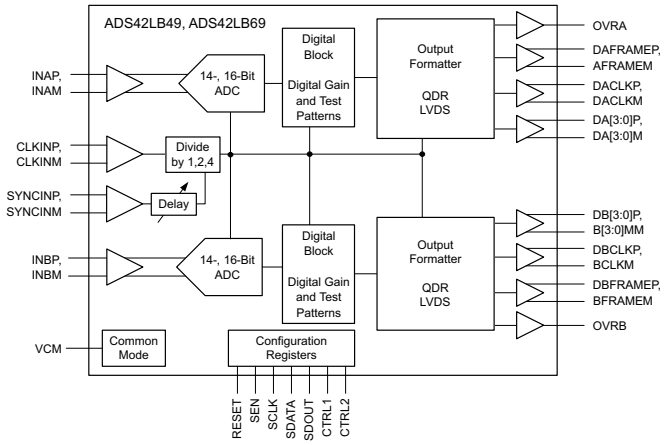
Dual-Channel, 14- and 16-Bit, 250-MSPS Analog-to-Digital Converters

Check for Samples: ADS42LB49, ADS42LB69

FEATURES

- **Dual Channel**
- **14- and 16-Bit Resolution**
- **Maximum Clock Rate: 250 MSPS**
- **Analog Input Buffer with High Impedance Input**
- **Flexible Input Clock Buffer with Divide-by-1, -2, and -4**
- **2-V_{PP} and 2.5-V_{PP} Differential Full-Scale Input (SPI-Programmable)**
- **DDR or QDR LVDS Interface**
- **64-Pin QFN Package (9-mm x 9-mm)**
- **Power Dissipation: 820 mW/ch**
- **Aperture Jitter: 85 f_S**
- **Internal Dither**
- **Channel Isolation: 100 dB**
- **Performance at f_{IN} = 170 MHz at 2 V_{PP}, –1 dBFS**
  - **SNR: 73.2 dBFS**
  - **SFDR:**
    - **87 dBc (HD2 and HD3)**
    - **100 dBc (Non HD2 and HD3)**
- **Performance at f_{IN} = 170 MHz: 2.5 V_{PP}, –1 dBFS**
  - **SNR: 74.9 dBFS**
  - **SFDR:**
    - **85 dBc (HD2 and HD3)**
    - **97 dBc (Non HD2 and HD3)**



APPLICATIONS

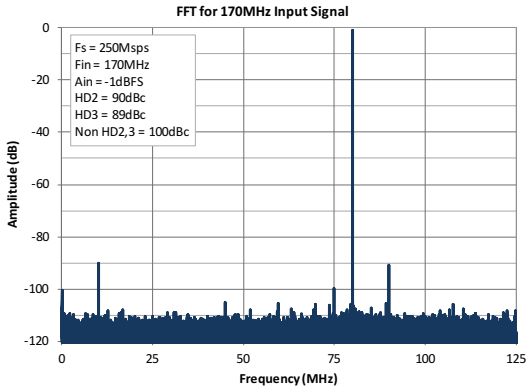
- **Communication and Cable Infrastructure**
- **Multi-Carrier, Multimode Cellular Receivers**
- **Radar and Smart Antenna Arrays**
- **Broadband Wireless**
- **Test and Measurement Systems**
- **Software-Defined and Diversity Radios**
- **Microwave and Dual-Channel I/Q Receivers**
- **Repeaters**
- **Power Amplifier Linearization**

DESCRIPTION

The ADS42LB49 and ADS42LB69 are a family of high-linearity, dual-channel, 14- and 16-bit, 250-MSPS, analog-to-digital converters (ADCs) supporting DDR and QDR LVDS output interfaces. The buffered analog input provides uniform input impedance across a wide frequency range while minimizing sample-and-hold glitch energy. A sampling clock divider allows more flexibility for system clock architecture design. The ADS42LB49 and ADS42LB69 provide excellent spurious-free dynamic range (SFDR) over a large input frequency range with low-power consumption.

Table 1. Family Comparison

INTERFACE OPTION	14-BIT	16-BIT
DDR, QDR LVDS	ADS42LB49	ADS42LB69
JESD204B	ADS42JB49	ADS42JB69



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range, unless otherwise noted.

		VALUE		UNIT
		MIN	MAX	
Supply voltage range	AVDD3V	–0.3	3.6	V
	AVDD	–0.3	2.1	V
	DRVDD	–0.3	2.1	V
Voltage between AGND and DGND		–0.3	0.3	V
Voltage applied to input pins	INA, INBP, INA, INBM	–0.3	3	V
	CLKINP, CLKINM	–0.3	AVDD + 0.3	V
	SYNCINP, SYNCINM	–0.3	AVDD + 0.3	V
	SCLK, SEN, SDATA, RESET, CTRL1, CTRL2	–0.3	3.9	V
Temperature range	Operating free-air, T_A	–40	+85	°C
	Operating junction, T_J		+125	°C
	Storage, T_{stg}	–65	+150	°C
Electrostatic discharge (ESD) ratings	Human body model (HBM)		2	kV

THERMAL INFORMATION

THERMAL METRIC(1)		ADS42LB49, ADS42LB69 RGC (QFN) 64 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	22.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	7.1	
θ_{JB}	Junction-to-board thermal resistance	2.5	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	2.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	0.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS(1)

Over operating free-air temperature range, unless otherwise noted.

PARAMETER			MIN	NOM	MAX	UNIT
SUPPLIES						
AVDD	Analog supply voltage		1.7	1.8	1.9	V
AVDD3V	Analog buffer supply voltage		3.15	3.3	3.45	V
DRVDD	Digital supply voltage		1.7	1.8	1.9	V
ANALOG INPUTS						
V_{ID}	Differential input voltage range	Default after reset		2		V_{PP}
		Register programmable(2)		2.5		V_{PP}
V_{ICR}	Input common-mode voltage			VCM ± 0.025		V
	Maximum analog input frequency with 2.5-V_{PP} input amplitude			250		MHz
	Maximum analog input frequency with 2-V_{PP} input amplitude			400		MHz
CLOCK INPUT						
	Input clock sample rate	QDR interface	30		250	MSPS
		DDR interface	10		250	MSPS
	Input clock amplitude differential (V_{CLKP} – V_{CLKM})	Sine wave, ac-coupled	0.3(3)	1.5		V_{PP}
		LVPECL, ac-coupled		1.6		V_{PP}
		LVDS, ac-coupled		0.7		V_{PP}
		LVCMOS, single-ended, ac-coupled		1.5		V
	Input clock duty cycle		35%	50%	65%	
DIGITAL OUTPUTS						
C_{LOAD}	Maximum external load capacitance from each output pin to DRGND			3.3		pF
R_{LOAD}	Single-ended load resistance			+50		Ω
T_A	Operating free-air temperature		–40		+85	°C

(1) After power-up, to reset the device for the first time, *only use the RESET pin*. Refer to the *Register Initialization* section.
(2) For details, refer to the *Digital Gain* section.
(3) Refer to the *Performance vs Clock Amplitude* curves, Figure 37 and Figure 38.

Table 2. High-Frequency Modes Summary

REGISTER ADDRESS	VALUE	DESCRIPTION
Dh	90h	Enable high-frequency modes for input frequencies greater than 250 MHz.
Eh	90h	Enable high-frequency modes for input frequencies greater than 250 MHz.

ELECTRICAL CHARACTERISTICS: ADS42LB69 (16-Bit)

Typical values are at T_A = +25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, and sampling rate = 250 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	2-V_{PP} FULL-SCALE			2.5-V_{PP} FULL-SCALE			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		73.9			75.8		dBFS
		f_{IN} = 70 MHz		73.7			75.5		dBFS
		f_{IN} = 170 MHz	70.8	73.2			74.7		dBFS
		f_{IN} = 230 MHz		72.8			74.1		dBFS
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		73.7			75.1		dBFS
		f_{IN} = 70 MHz		73.6			75.3		dBFS
		f_{IN} = 170 MHz	69.6	73.1			74.2		dBFS
		f_{IN} = 230 MHz		72.5			73.4		dBFS
SFDR	Spurious-free dynamic range (including second and third harmonic distortion)	f_{IN} = 10 MHz		87			83		dBc
		f_{IN} = 70 MHz		90			88		dBc
		f_{IN} = 170 MHz	81	87			85		dBc
		f_{IN} = 230 MHz		86			83		dBc
THD	Total harmonic distortion	f_{IN} = 10 MHz		86			82		dBc
		f_{IN} = 70 MHz		89			87		dBc
		f_{IN} = 170 MHz	78	85			82		dBc
		f_{IN} = 230 MHz		83			81		dBc
HD2	2nd-order harmonic distortion	f_{IN} = 10 MHz		97			95		dBc
		f_{IN} = 70 MHz		90			88		dBc
		f_{IN} = 170 MHz	81	87			85		dBc
		f_{IN} = 230 MHz		86			84		dBc
HD3	3rd-order harmonic distortion	f_{IN} = 10 MHz		87			83		dBc
		f_{IN} = 70 MHz		96			94		dBc
		f_{IN} = 170 MHz	81	91			85		dBc
		f_{IN} = 230 MHz		87			83		dBc
	Worst spur (other than second and third harmonics)	f_{IN} = 10 MHz		102			103		dBc
		f_{IN} = 70 MHz		101			103		dBc
		f_{IN} = 170 MHz	87	101			101		dBc
		f_{IN} = 230 MHz		100			100		dBc
IMD	Two-tone intermodulation distortion	f_1 = 46 MHz, f_2 = 50 MHz, each tone at –7 dBFS		97			94		dBFS
		f_1 = 185 MHz, f_2 = 190 MHz, each tone at –7 dBFS		94			90		dBFS
	Crosstalk	20-MHz, full-scale signal on channel under observation; 170-MHz, full-scale signal on other channel		100			100		dB
	Input overload recovery	Recovery to within 1% (of full-scale) for 6-dB overload with sine-wave input		1			1		Clock cycle
PSRR	AC power-supply rejection ratio	For 50-mV_{PP} signal on AVDD supply, up to 10 MHz		> 40			> 40		dB
ENOB	Effective number of bits	f_{IN} = 170 MHz		11.85			12.03		LSBs
DNL	Differential nonlinearity	f_{IN} = 170 MHz		±0.6			±0.6		LSBs
INL	Integrated nonlinearity	f_{IN} = 170 MHz		±3	±8		±3.5		LSBs

ELECTRICAL CHARACTERISTICS: ADS42LB49 (14-Bit)

Typical values are at T_A = +25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, and sampling rate = 250 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	2-V_{PP} FULL-SCALE			2.5-V_{PP} FULL-SCALE			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-noise ratio	f_{IN} = 10 MHz		73.3			74.9		dBFS
		f_{IN} = 70 MHz		73.1			74.7		dBFS
		f_{IN} = 170 MHz	69.5	72.7			74.1		dBFS
		f_{IN} = 230 MHz		72.3			73.5		dBFS
SINAD	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		73.1			74.1		dBFS
		f_{IN} = 70 MHz		73.1			74.4		dBFS
		f_{IN} = 170 MHz	68.5	72.6			73.6		dBFS
		f_{IN} = 230 MHz		72			72.9		dBFS
SFDR	Spurious-free dynamic range (including second and third harmonic distortion)	f_{IN} = 10 MHz		87			82		dBc
		f_{IN} = 70 MHz		90			88		dBc
		f_{IN} = 170 MHz	79	87			85		dBc
		f_{IN} = 230 MHz		86			83		dBc
THD	Total harmonic distortion	f_{IN} = 10 MHz		86			81		dBc
		f_{IN} = 70 MHz		89			87		dBc
		f_{IN} = 170 MHz	76	85			82		dBc
		f_{IN} = 230 MHz		83			81		dBc
HD2	2nd-order harmonic distortion	f_{IN} = 10 MHz		97			95		dBc
		f_{IN} = 70 MHz		90			88		dBc
		f_{IN} = 170 MHz	79	87			85		dBc
		f_{IN} = 230 MHz		86			84		dBc
HD3	3rd-order harmonic distortion	f_{IN} = 10 MHz		87			82		dBc
		f_{IN} = 70 MHz		96			94		dBc
		f_{IN} = 170 MHz	79	91			85		dBc
		f_{IN} = 230 MHz		87			83		dBc
	Worst spur (other than second and third harmonics)	f_{IN} = 10 MHz		104			103		dBc
		f_{IN} = 70 MHz		101			103		dBc
		f_{IN} = 170 MHz	87	100			101		dBc
		f_{IN} = 230 MHz		99			100		dBc
IMD	Two-tone intermodulation distortion	f_1 = 46 MHz, f_2 = 50 MHz, each tone at –7 dBFS		99			95		dBFS
		f_1 = 185 MHz, f_2 = 190 MHz, each tone at –7 dBFS		93			93		dBFS
	Crosstalk	20-MHz, full-scale signal on channel under observation; 170-MHz, full-scale signal on other channel		100			90		dB
	Input overload recovery	Recovery to within 1% (of full-scale) for 6-dB overload with sine-wave input		1			1		Clock cycle
PSRR	AC power-supply rejection ratio	For a 50-mV_{PP} signal on AVDD supply, up to 10 MHz		> 40			> 40		dB
ENOB	Effective number of bits	f_{IN} = 170 MHz		11.76			11.93		LSBs
DNL	Differential nonlinearity	f_{IN} = 170 MHz		±0.15			±0.15		LSBs
INL	Integrated nonlinearity	f_{IN} = 170 MHz		±0.75	±3		±0.9		LSBs

ELECTRICAL CHARACTERISTICS: General

Typical values are at +25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, 50% clock duty cycle, –1-dBFS differential analog input, and sampling rate = 250 MSPS, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
V_{ID}	Differential input voltage range	Default (after reset)		2		V_{PP}
		Register programmed (1)		2.5		V_{PP}
		Differential input resistance (at 170 MHz)		1.2		kΩ
		Differential input capacitance (at 170 MHz)		4		pF
	Analog input bandwidth	With 50-Ω source impedance, and 50-Ω termination		900		MHz
VCM	Common-mode output voltage			1.9		V
	VCM output current capability			10		mA
DC ACCURACY						
	Offset error		–20		20	mV
E_{GREF}	Gain error as a result of internal reference inaccuracy alone			±2		%FS
E_{GCHAN}	Gain error of channel alone			–5		%FS
	Temperature coefficient of E_{GCHAN}			0.01		Δ%/°C
POWER SUPPLY						
IAVDD	Analog supply current			141	182	mA
IAVDD3V	Analog buffer supply current			302	340	mA
IDRVDD	Digital and Output buffer supply current	External 100-Ω differential termination on LVDS outputs		219	245	mA
	Analog power			253		mW
	Analog buffer power			996		mW
	Power consumption (includes digital blocks and output buffers)	External 100-Ω differential termination on LVDS outputs		393		mW
	Total power			1.64	1.85	W
	Global power-down (both channels)				160	mW

(1) Refer to the *Serial Interface* section.

TIMING REQUIREMENTS: General

Typical values are at +25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, sampling frequency = 250 MSPS, sine wave input clock, C_{LOAD} = 3.3 pF, and R_{LOAD} = 100 Ω, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.7 V to 1.9 V.

PARAMETER		DESCRIPTION	MIN	TYP	MAX	UNIT
t_A	Aperture delay		0.5	0.7	1.1	ns
	Aperture delay matching	Between two channels of the same device		±70		ps
	Variation of aperture delay	Between two devices at the same temperature and supply voltage.		±150		ps
t_J	Aperture jitter			85		f_S rms
	Wakeup time	Time to valid data after coming out of STANDBY mode		50	100	µs
		Time to valid data after coming out of GLOBAL power-down mode (in this mode, both channels power-down)		250	1000	µs
	ADC latency(1)	Default latency after reset		14		Clock cycles
		Normal OVR latency		14		Clock cycles
		Fast OVR latency		9		Clock cycles
t_{SU_SYNCIN}		Setup time for SYNCIN Referenced to input clock rising edge	400			ps
t_{H_SYNCIN}		Hold time for SYNCIN Referenced to input clock rising edge	100			ps

(1) Overall latency = ADC latency + t_{PDI}.

TIMING DIAGRAM: General

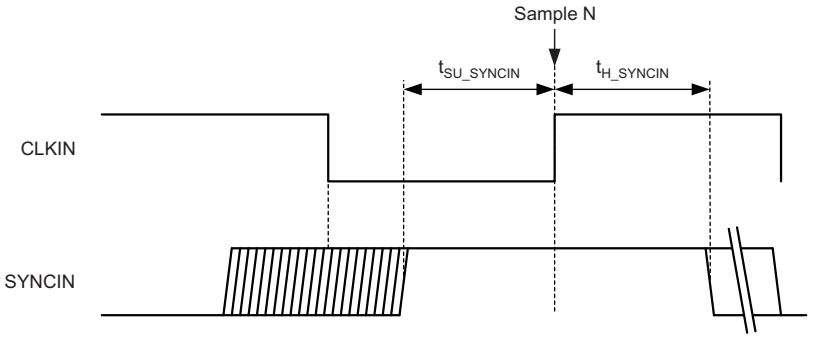


Figure 1. Timing Diagram for SYNCINP and SYNCINM Inputs

TIMING REQUIREMENTS: DDR LVDS Mode(1)

Typical values are at +25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, sampling frequency = 250 MSPS, sine wave input clock, C_{LOAD} = 3.3 pF, and R_{LOAD} = 100 Ω, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, and DRVDD = 1.7 V to 1.9 V.

PARAMETER		DESCRIPTION	MIN	TYP	MAX	UNIT
t_{SU}	Data setup time	Data valid to zero-crossing of differential output clock (CLKOUTP – CLKOUTM)(2)	0.62	0.82		ns
t_{HO}	Data hold time	Zero-crossing of differential output clock (CLKOUTP – CLKOUTM) to data becoming invalid(2)	0.54	0.64		ns
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output clock (CLKOUTP – CLKOUTM) rising edge cross-over	8	10.5	13	ns
	LVDS bit clock duty cycle	Duty cycle of differential clock (CLKOUTP – CLKOUTM)		52		%
t_{FALL}, t_{RISE}	Data fall time, Data rise time	Rise time measured from –100 mV to +100 mV *10 MSPS ≤ Sampling frequency ≤ 250 MSPS*		0.14		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, Output clock fall time	Rise time measured from –100 mV to +100 mV *10 MSPS ≤ Sampling frequency ≤ 250 MSPS*		0.18		ns

(1) Measurements are done with a transmission line of a 100-Ω characteristic impedance between the device and load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(2) Data valid refers to a logic high of +100 mV and a logic low of –100 mV.

Table 3. DDR LVDS Timings at Lower Sampling Frequencies

SAMPLING FREQUENCY (MSPS)	SETUP TIME (ns)			HOLD TIME (ns)			CLOCK PROPAGATION DELAY (ns)		
	t_{SU}			t_{HO}			t_{PDI}		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
80	2.40	2.96		2.16	2.82		9	11.9	15
120	1.57	1.92		1.40	1.84		8	11.1	14
160	1.17	1.40		1.02	1.36		8	10.6	13
200	0.82	1.07		0.72	1.02		8	10.5	13
230	0.69	0.91		0.61	0.84		8	10.5	13

TIMING DIAGRAM: DDR LVDS Mode

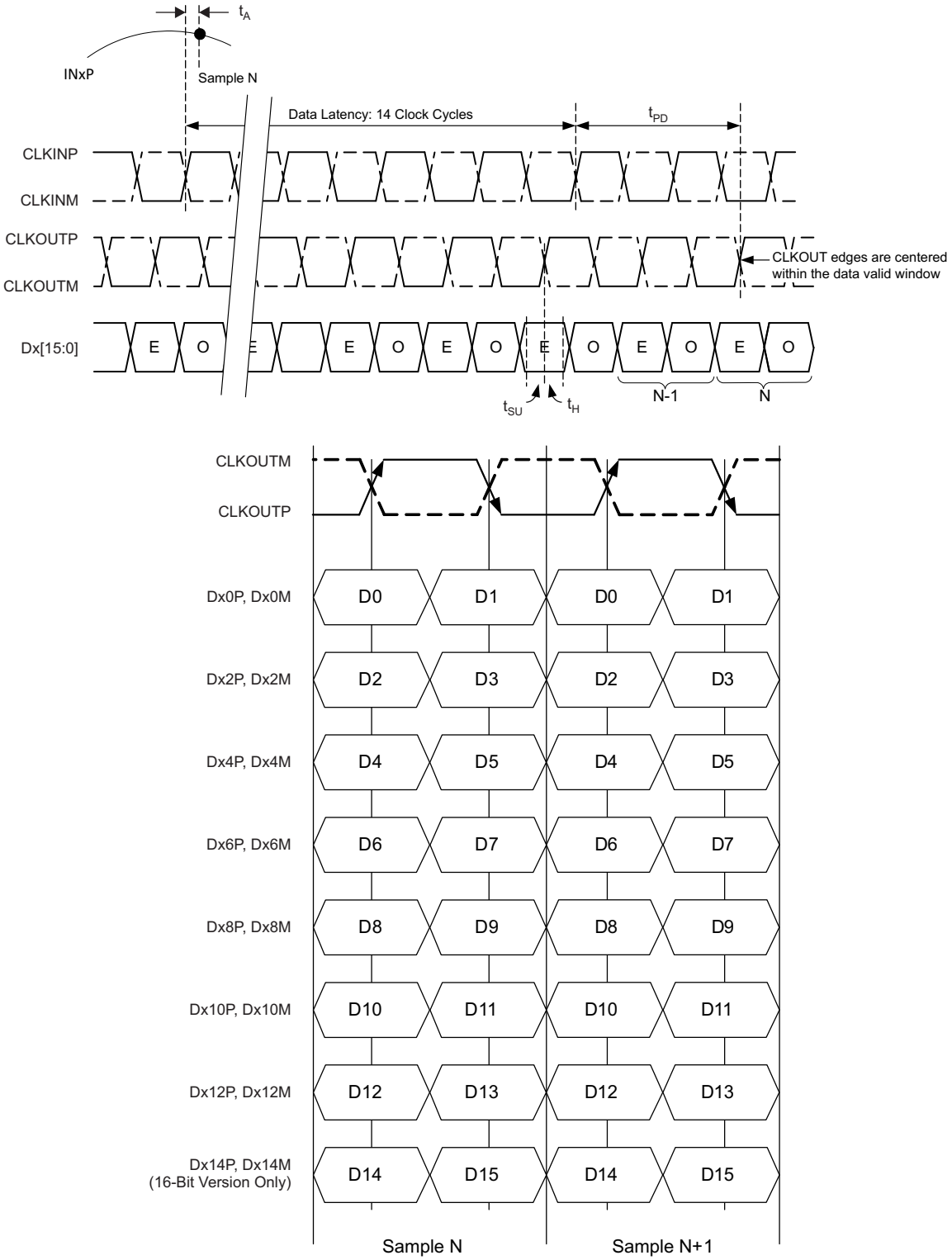


Figure 2. DDR LVDS Output Timing Diagram

TIMING REQUIREMENTS: QDR LVDS Mode(1)(2)

Typical values are at +25°C, AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, sampling frequency = 250 MSPS, sine-wave input clock, C_{LOAD} = 3.3 pF(3), and R_{LOAD} = 100 Ω(4), unless otherwise noted. Minimum and maximum values are across the full temperature range of T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD = 1.8 V, AVDD3V = 3.3 V, and DRVDD = 1.7 V to 1.9 V.

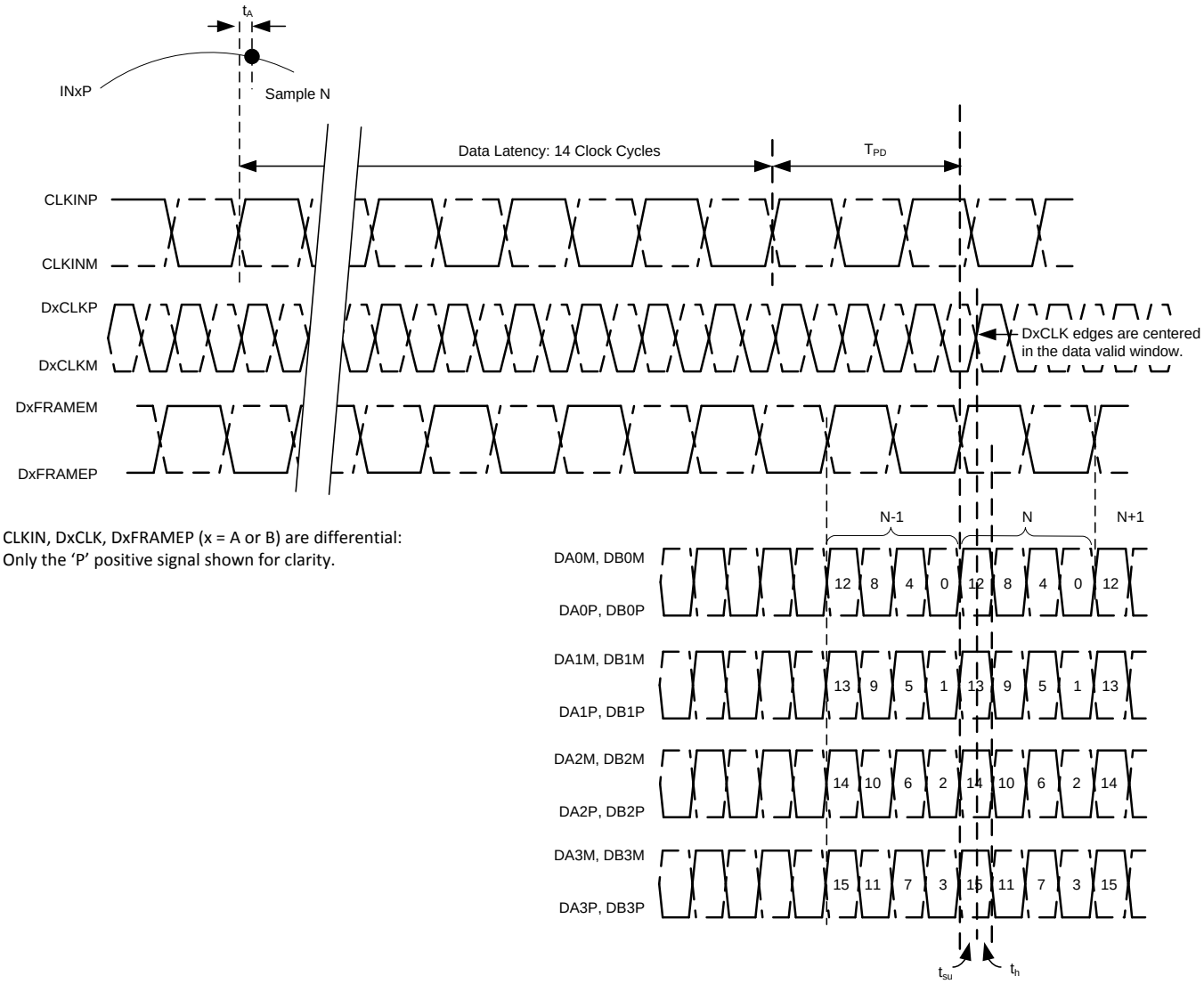
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SU}	Data setup time(5)(6)	Data valid to DxCLKP, DxCLKM zero-crossing	0.23	0.31		ns
t_H	Data hold time(5)(6)	DxCLKP, DxCLKM zero-crossing to data becoming invalid	0.16	0.29		ns
	LVDS bit clock duty cycle	Differential bit clock duty cycle (DxCLKP, DxCLKM)		50%		
t_{PDI}	Clock propagation delay	Input clock rising edge cross-over to output frame clock (DxFRAMEP-DxFRAMEM) rising edge cross-over	7	10.1	13	ns
t_{RISE}, t_{FALL}	Data rise and fall time	Rise time measured from –100 mV to +100 mV		0.18		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise and fall time	Rise time measured from –100 mV to +100 mV		0.2		ns

(1) Measurements are done with a transmission line of 100-Ω characteristic impedance between the device and load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(2) Timing parameters are ensured by design and characterization and are not tested in production.
(3) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground.
(4) R_{LOAD} is the differential load resistance between the LVDS output pair.
(5) Data valid refers to a logic high of +100 mV and a logic low of –100 mV.
(6) The setup and hold times of a channel are measured with respect to the same channel output clock.

Table 4. QDR LVDS Timings at Lower Sampling Frequencies

SAMPLING FREQUENCY (MSPS)	SETUP TIME (ns)			HOLD TIME (ns)			CLOCK PROPAGATION DELAY (ns)		
	t_{SU}			t_{HO}			t_{PDI}		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
80	1.06	1.21		0.84	1.29		6	9.3	12
120	0.63	0.77		0.66	0.88		7	9.5	13
160	0.43	0.55		0.39	0.61		7	9.7	13
200	0.31	0.42		0.28	0.47		7	9.8	13
230	0.24	0.34		0.17	0.36		7	9.9	13

TIMING DIAGRAM: QDR LVDS Mode



CLKIN, DxCLK, DxFRAMEP (x = A or B) are differential:
Only the 'P' positive signal shown for clarity.

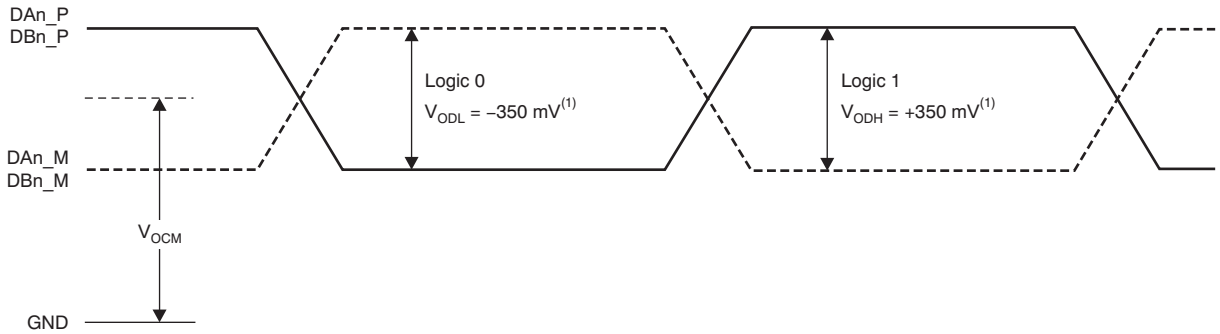
Figure 3. QDR LVDS Output Timing Diagram

DIGITAL CHARACTERISTICS

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level '0' or '1'. AVDD = 1.8 V, AVDD3V = 3.3 V, DRVDD = 1.8 V, and, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS (RESET, SCLK, SDATA, SEN, CTRL1, CTRL2)(1)							
V_{IH}	High-level input voltage		All digital inputs support 1.8-V and 3.3-V CMOS logic levels	1.3			V
V_{IL}	Low-level input voltage					0.4	V
I_{IH}	High-level input current	RESET, SDATA, SCLK, CTRL1, CTRL2(2)	V_{HIGH} = 1.8 V		10		µA
		SEN(3)	V_{HIGH} = 1.8 V		0		µA
I_{IL}	Low-level input current	RESET, SDATA, SCLK, CTRL1, CTRL2	V_{LOW} = 0 V		0		µA
		SEN	V_{LOW} = 0 V		10		µA
DIGITAL OUTPUTS, CMOS INTERFACE (OVRA, OVRB, SDOUT)							
V_{OH}	High-level output voltage			DRVDD – 0.1	DRVDD		V
V_{OL}	Low-level output voltage				0	0.1	V
DIGITAL OUTPUTS, LVDS INTERFACE							
V_{ODH}	High-level output differential voltage		With an external 100-Ω termination	250	350	500	mV
V_{ODL}	Low-level output differential voltage		With an external 100-Ω termination	–500	–350	–250	mV
V_{OCM}	Output common-mode voltage				1.05		V

(1) SCLK, SDATA, and SEN function as digital input pins in serial configuration mode.
(2) SDATA and SCLK have an internal 150-kΩ pull-down resistor.
(3) SEN has an internal 150-kΩ pull-up resistor to AVDD. Because the pull-up resistor is weak, SEN can also be driven by 1.8-V or 3.3-V CMOS buffers.



(1) With an external 100-Ω termination.

Figure 4. DDR LVDS Output Voltage Levels

PIN CONFIGURATIONS

RGC PACKAGE
QFN-64
(Top View)

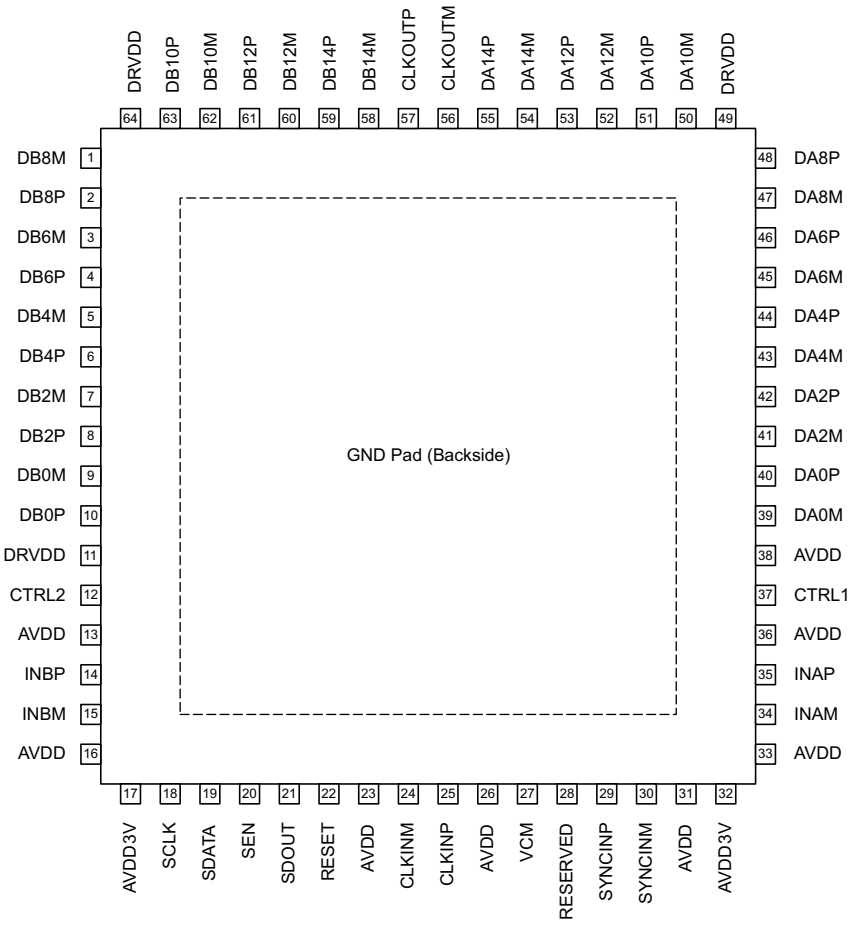


Figure 5. ADS42LB69 DDR LVDS

PIN ASSIGNMENTS: ADS42LB69 DDR LVDS OUTPUT INTERFACE

PIN		I/O	DESCRIPTION
NAME	NUMBER		
INPUT AND REFERENCE			
INAP, INAM	36, 35	I	Differential analog input for channel A
INBP, INBM	14, 15	I	Differential analog input for channel B
VCM	27	O	Common-mode voltage for analog inputs, 1.9 V
CLOCK AND SYNC			
CLKINP, CLKINM	25, 24	I	Differential clock input for ADC
SYNCINP, SYNCINM	29, 30	I	External sync input. If not used, connect SYNCINP to GND and SYNCINM to AVDD.
CONTROL AND SERIAL			
CTRL1	37	I/O	Can be configured as power-down input pin or as OVR output pin for channel A, depending on the register bit PDN/OVR FOR CTRL PINS.
CTRL2	12	I/O	Can be configured as power-down input pin or as OVR output pin for channel B, depending on the register bit PDN/OVR FOR CTRL PINS
Reserved	28	—	Do not connect
RESET	22	I	Hardware reset. Active high.
SCLK	18	I	Serial interface clock input
SDATA	19	I	Serial interface data input.
SDOUT	21	O	Serial interface data output
SEN	20	I	Serial interface enable
DATA INTERFACE			
CLKOUTP, CLKOUTM	57, 56	O	Differential LVDS output clock
DA[14:0]P, DA[14:0]M	39-48, 50-55	O	DDR LVDS output interface for channel A
DB[14:0]P, DB[14:0]M	1-10, 58-63	O	DDR LVDS output interface for channel B
POWER SUPPLY			
AVDD	13, 16, 23, 26, 31, 33, 36, 38	I	Analog 1.8-V power supply
AVDD3V	17, 32	I	Analog 3.3 V power supply for analog buffer
DRVDD	11, 49, 64	I	Digital 1.8-V power supply
GND	Ground pad	I	Ground

RGC PACKAGE
QFN-64
(Top View)

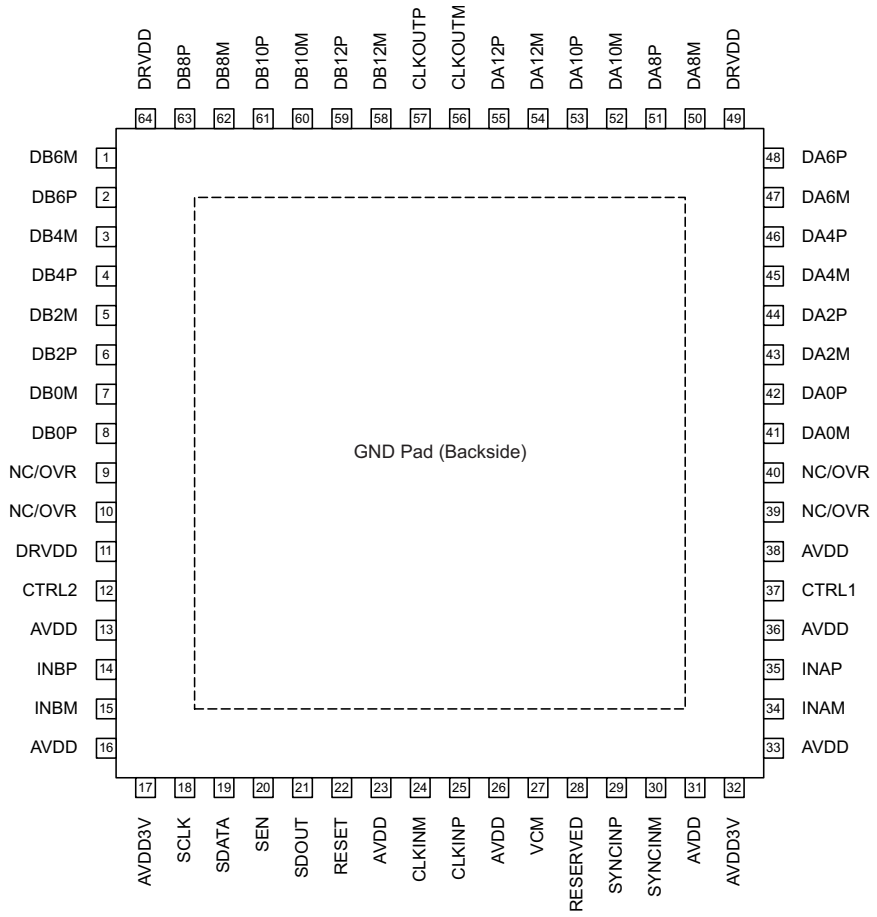


Figure 6. ADS42LB49 DDR LVDS

PIN ASSIGNMENTS: ADS42LB49 DDR LVDS OUTPUT INTERFACE

PIN		I/O	DESCRIPTION
NAME	NUMBER		
INPUT AND REFERENCE			
INAP, INAM	35, 35	I	Differential analog input for channel A
INBP, INBM	14, 15	I	Differential analog input for channel B
VCM	27	O	Common-mode voltage for analog inputs, 1.9 V
CLOCK AND SYNC			
CLKINP, CLKINM	25, 24	I	Differential clock input for ADC
SYNCINP, SYNCINM	29, 30	I	External sync input. If not used, connect SYNCINP to GND and SYNCINM to AVDD.
CONTROL AND SERIAL			
CTRL1	37	I/O	Can be configured as power-down input pin or as OVR output pin for channel A, depending on the register bit PDN/OVR FOR CTRL PINS.
CTRL2	12	I/O	Can be configured as power-down input pin or as OVR output pin for channel B, depending on the register bit PDN/OVR FOR CTRL PINS
NC/OVR	9, 10, 39, 40	—	If the OVR ON LSB bit is set, these pins can be used because they carry overrange information. Otherwise, do not connect these pins.
Reserved	28	—	Do not connect
RESET	22	I	Hardware reset. Active high.
SCLK	18	I	Serial interface clock input
SDATA	19	I	Serial interface data input.
SDOUT	21	O	Serial interface data output
SEN	20	I	Serial interface enable
DATA INTERFACE			
CLKOUTP, CLKOUTM	57, 56	O	Differential LVDS output clock
DA[14:0]P, DA[14:0]M	41-48, 50-55	O	DDR LVDS output interface for channel A
DB[14:0]P, DB[14:0]M	1-8, 58-63	O	DDR LVDS output interface for channel B
POWER SUPPLY			
AVDD	13, 16, 23, 26, 31, 33, 36, 38	I	Analog 1.8-V power supply
AVDD3V	17, 32	I	Analog 3.3-V analog supply for analog buffer
DRVDD	11, 49, 64	I	Digital 1.8-V power supply
GND	Ground pad	I	Ground

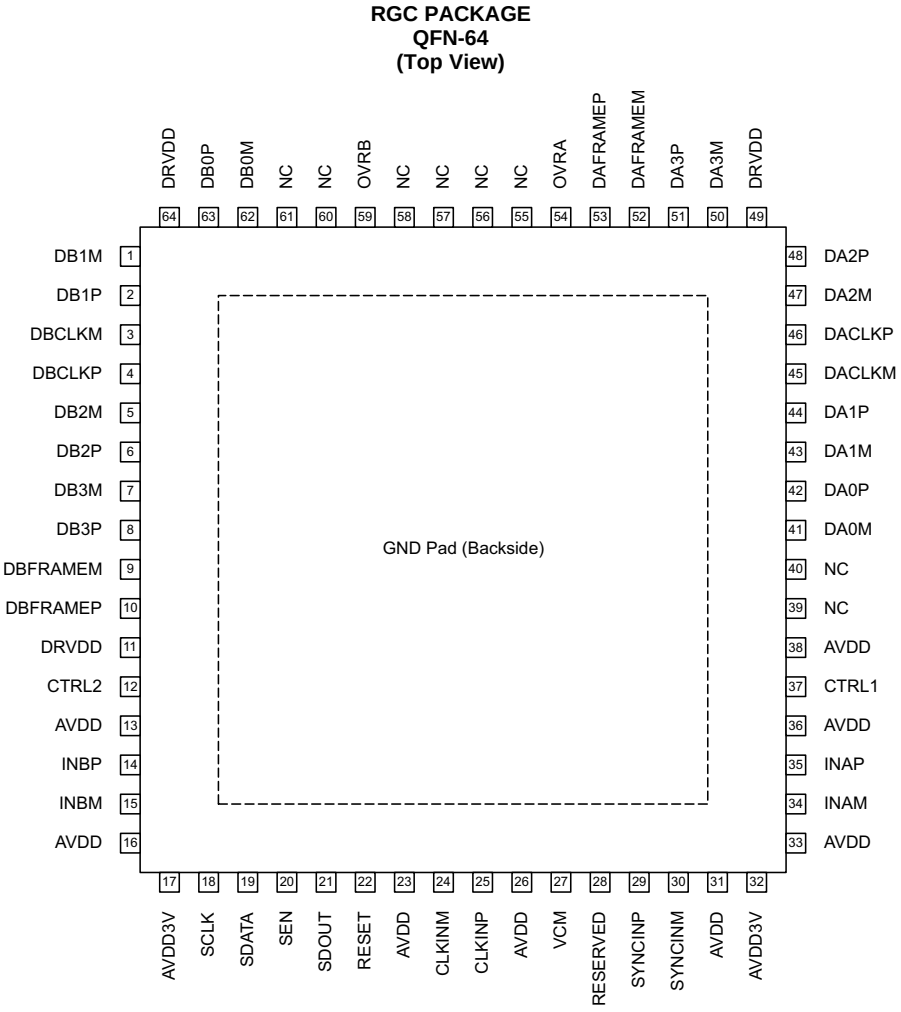


Figure 7. ADS42LB69, ADS42LB49 QDR LVDS

PIN ASSIGNMENTS: QDR LVDS OUTPUT INTERFACE

PIN		I/O	DESCRIPTION
NAME	NUMBER		
INPUT AND REFERENCE			
INAP, INAM	34, 35	I	Differential analog input for channel A
INBP, INBM	14, 15	I	Differential analog input for channel B
VCM	27	O	Common-mode voltage for analog inputs, 1.9 V
CLOCK AND SYNC			
CLKINP, CLKINM	24, 25	I	Differential clock input for ADC
SYNCINP, SYNCINM	29, 30	I	External sync input If not used, connect SYNCINP to GND and SYNCINM to AVDD.
CONTROL AND SERIAL			
CTRL1	37	I	Can be configured as power-down input pin or as OVR output pin for channel A, depending on the register bit PDN/OVR FOR CTRL PINS.
CTRL2	12	I	Can be configured as power-down input pin or as OVR output pin for channel B, depending on the register bit PDN/OVR FOR CTRL PINS
NC	39, 40, 55-58, 60, 61	—	Do not connect
Reserved	28	—	Do not connect
RESET	22	I	Hardware reset. Active high.
SCLK	18	I	Serial interface clock input
SDATA	19	I	Serial interface data input.
SDOUT	21	O	Serial interface data output
SEN	20	I	Serial interface enable
DATA INTERFACE			
DA[3:0]P, DA[3:0]M	41-44, 47, 48, 50, 51	O	4-bit QDR LVDS output interface for channel A
DACLKP, DACLKM	45, 46	O	Differential output clock for channel A
DAFRAMEP, DAFRAMEM	52, 53	—	Differential frame clock output for channel A
DB[3:0]P, DB[3:0]M	1, 2, 5-8, 62, 63	—	4-bit QDR LVDS output interface for channel B
DBCLKP, DBCLKM	3, 4	—	Differential output clock for channel A
DBFRAMEP, DBFRAMEM	9, 10	—	Differential frame clock output for channel A
OVRA	54	O	Overrange indication channel A
OVRB	59	O	Overrange indication channel A
POWER SUPPLY			
AVDD	13, 16, 23, 26, 31, 33, 36, 38	I	Analog 1.8-V power supply
AVDD3V	17, 32	I	Analog 3.3-V power supply for analog buffer
DRVDD	11, 49, 64	I	Digital 1.8-V power supply
GND	Ground pad	I	Ground

FUNCTIONAL BLOCK DIAGRAMS

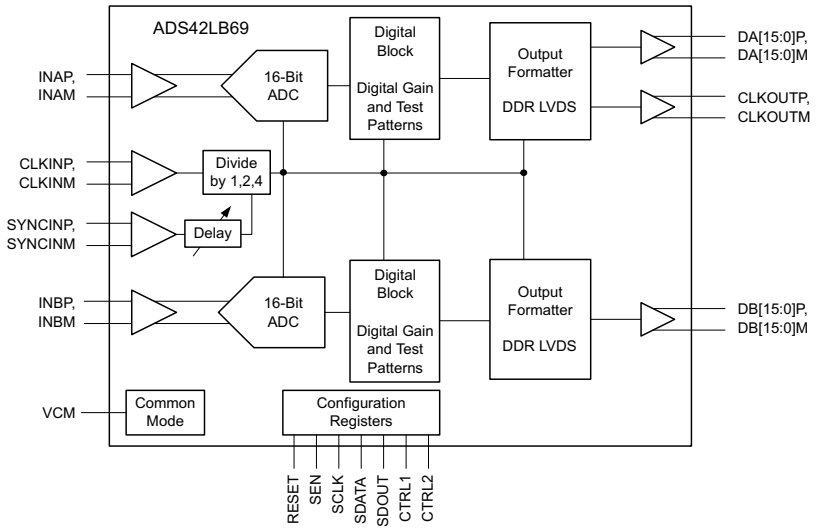


Figure 8. ADS42LB69 DDR LVDS

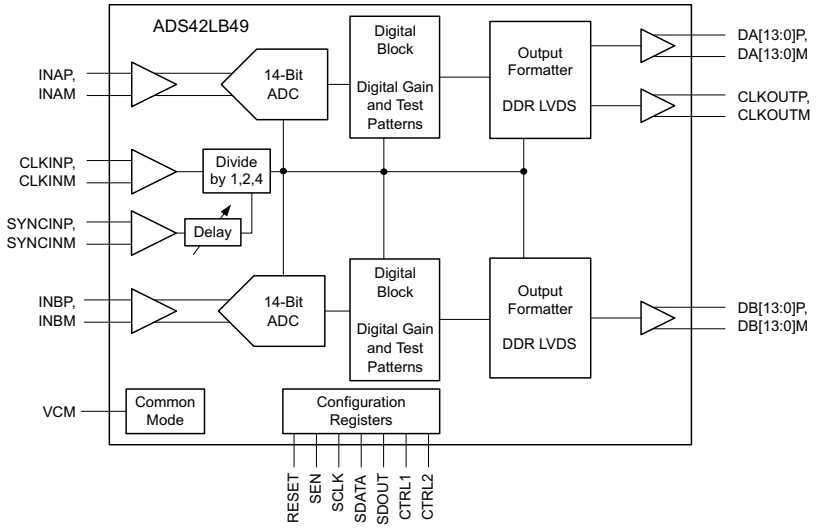


Figure 9. ADS42LB49 DDR LVDS

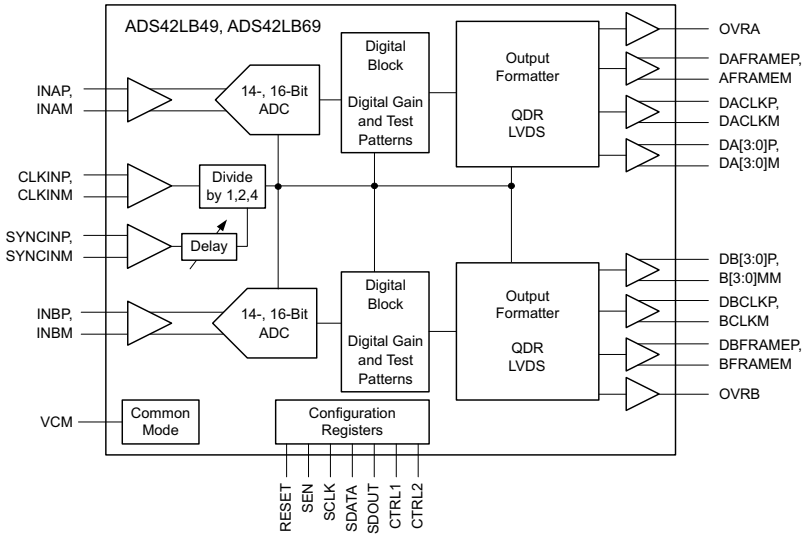


Figure 10. ADS42LB69, ADS42LB49 QDR LVDS

TYPICAL CHARACTERISTICS: ADS42LB69

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, QDR interface, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

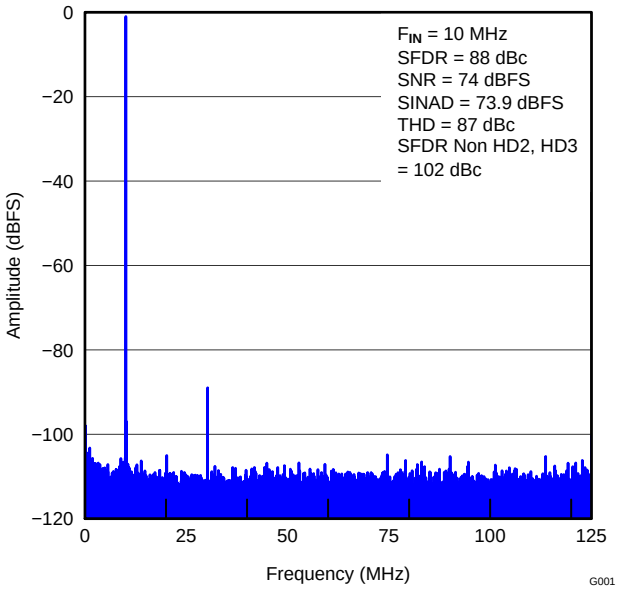


Figure 11. FFT FOR 10-MHz INPUT SIGNAL

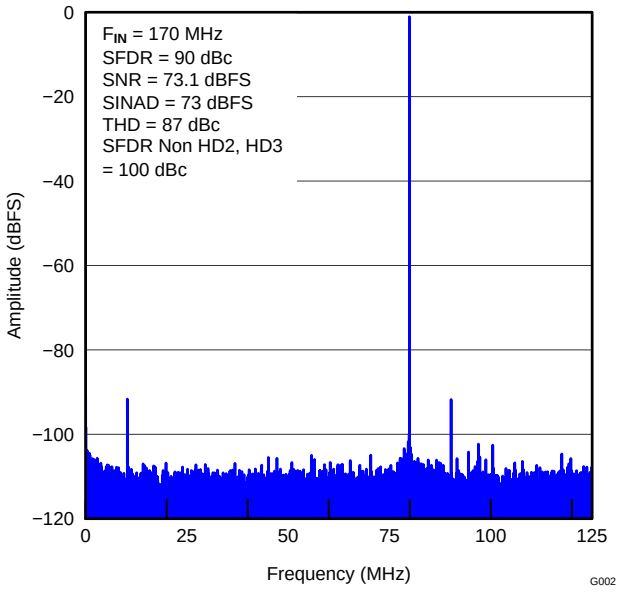


Figure 12. FFT FOR 170-MHz INPUT SIGNAL

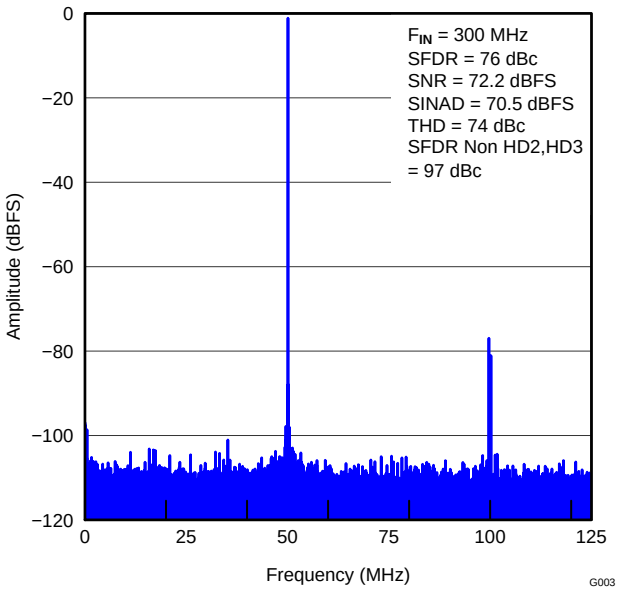


Figure 13. FFT FOR 300-MHz INPUT SIGNAL

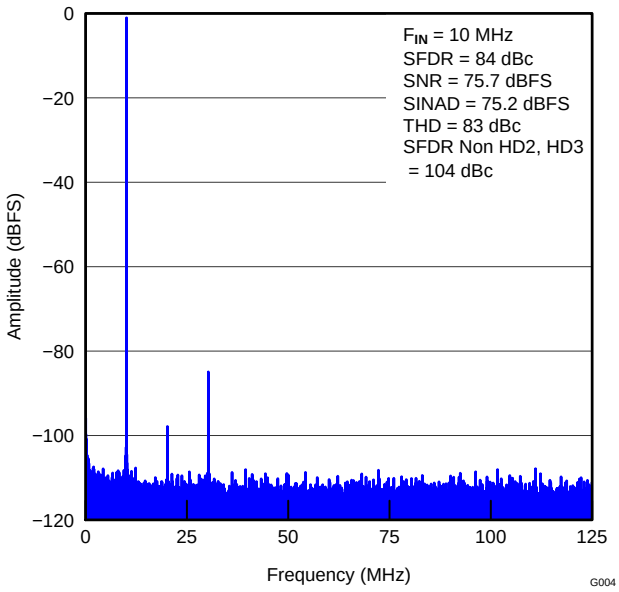


Figure 14. FFT FOR 10-MHz INPUT SIGNAL (2.5-V_{PP} Full-Scale)

TYPICAL CHARACTERISTICS: ADS42LB69 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, QDR interface, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

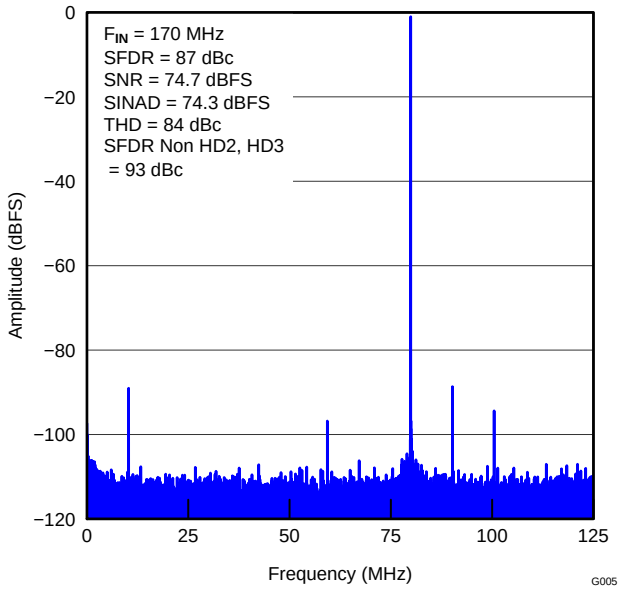


Figure 15. FFT FOR 170-MHz INPUT SIGNAL (2.5-V_{PP} Full-Scale)

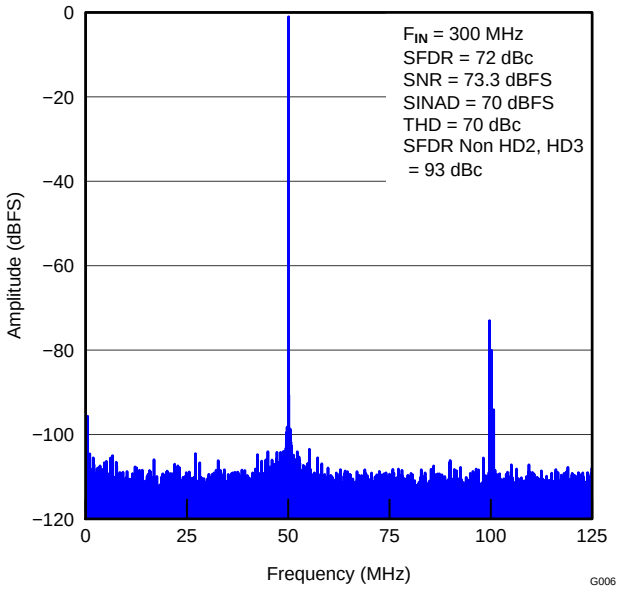


Figure 16. FFT FOR 300-MHz INPUT SIGNAL (2.5-V_{PP} Full-Scale)

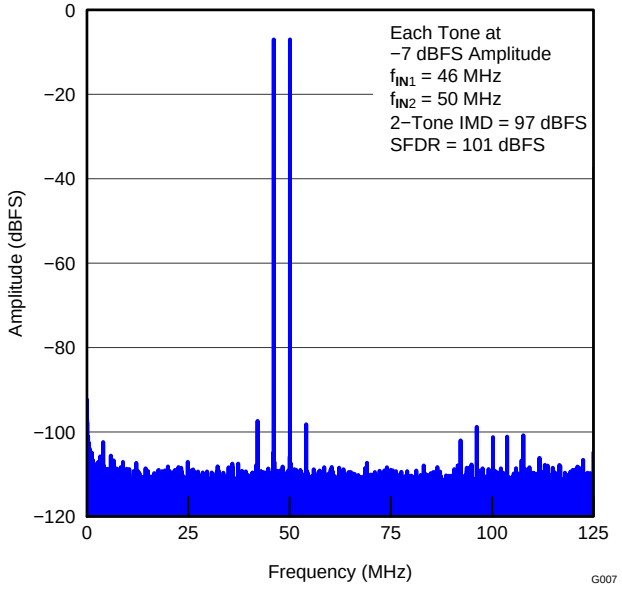


Figure 17. FFT FOR TWO-TONE INPUT SIGNAL (At –7 dBFS, 46 MHz and 50 MHz)

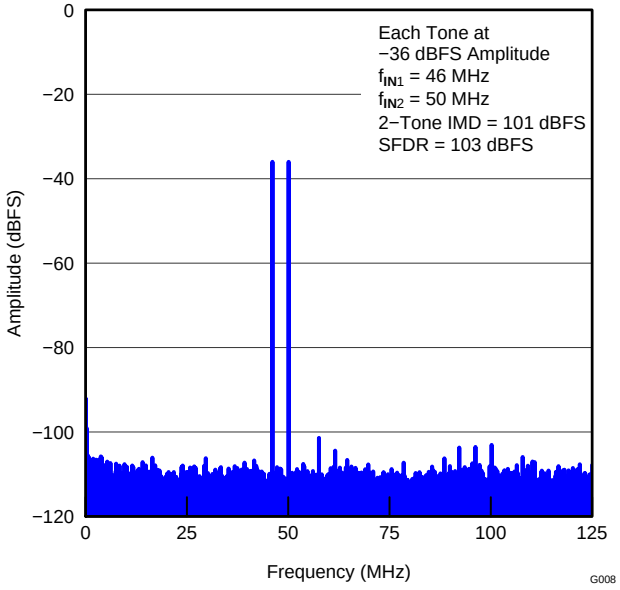


Figure 18. FFT FOR TWO-TONE INPUT SIGNAL (At –36 dBFS, 46 MHz and 50 MHz)

TYPICAL CHARACTERISTICS: ADS42LB69 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, QDR interface, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

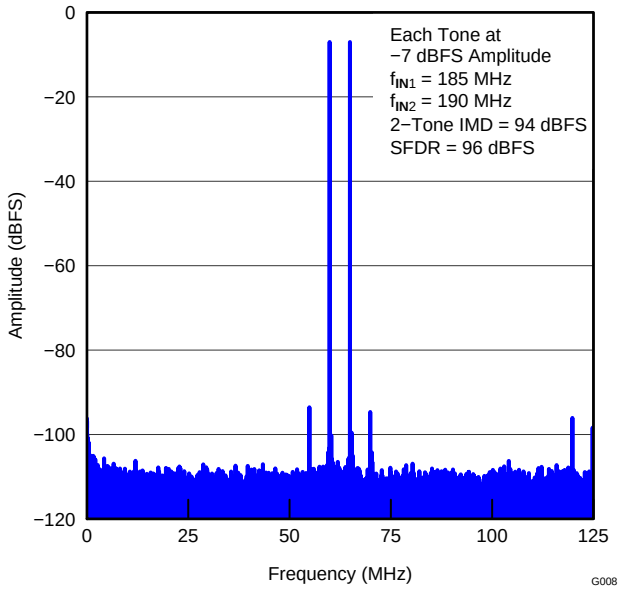


Figure 19. FFT FOR TWO-TONE INPUT SIGNAL (At –7 dBFS, 185 MHz and 190 MHz)

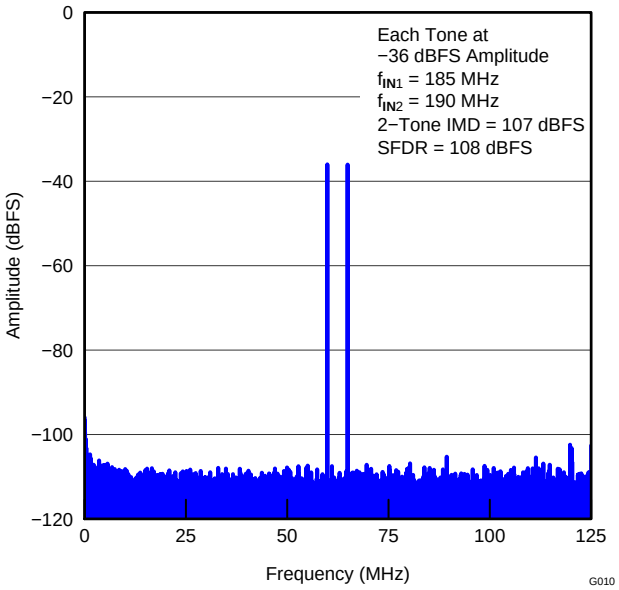


Figure 20. FFT FOR TWO-TONE INPUT SIGNAL (At –36 dBFS, 185 MHz and 190 MHz)

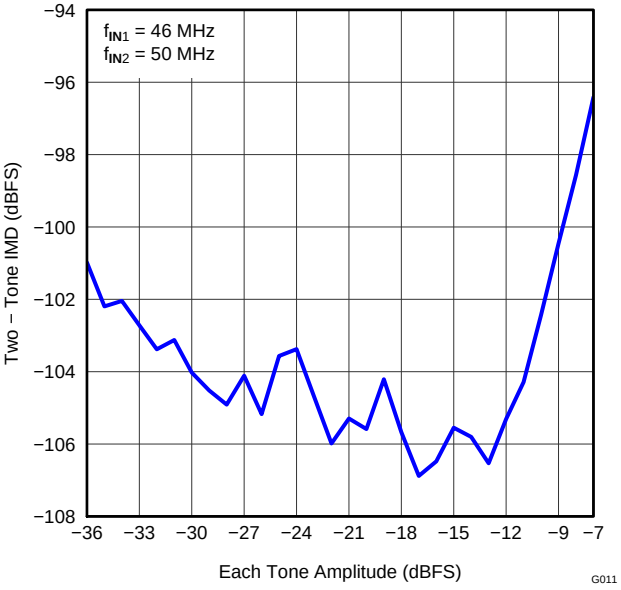


Figure 21. IMD3 vs INPUT AMPLITUDE (46 MHz and 50 MHz)

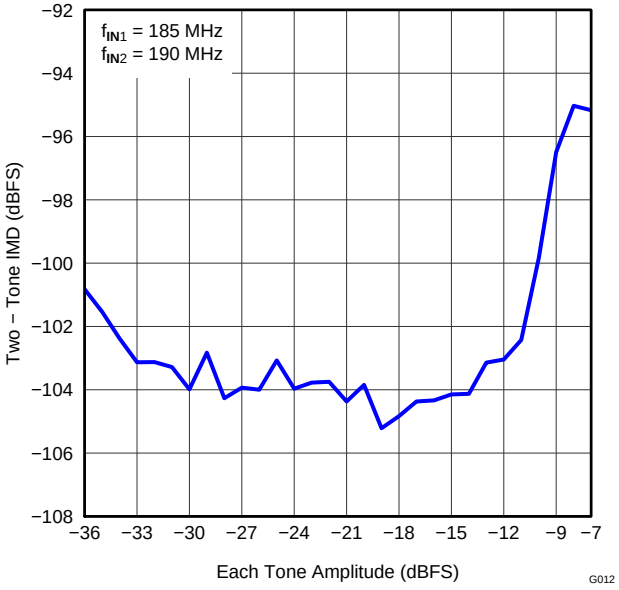


Figure 22. IMD3 vs INPUT AMPLITUDE (185 MHz and 190 MHz)

TYPICAL CHARACTERISTICS: ADS42LB69 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, QDR interface, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

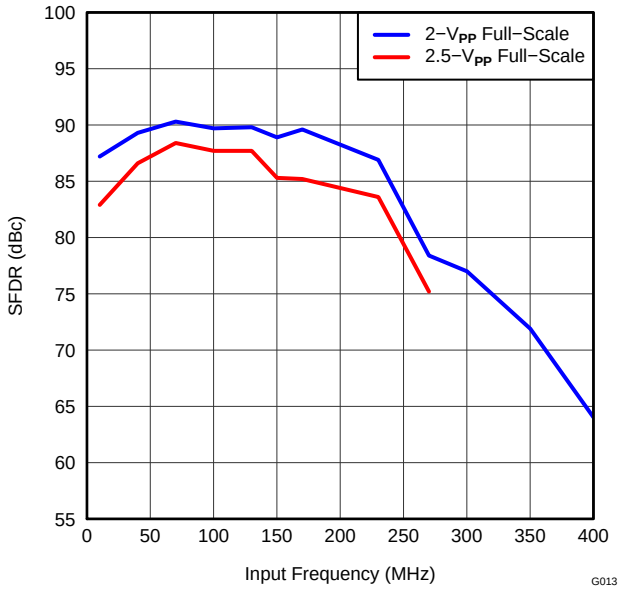


Figure 23. SFDR vs INPUT FREQUENCY

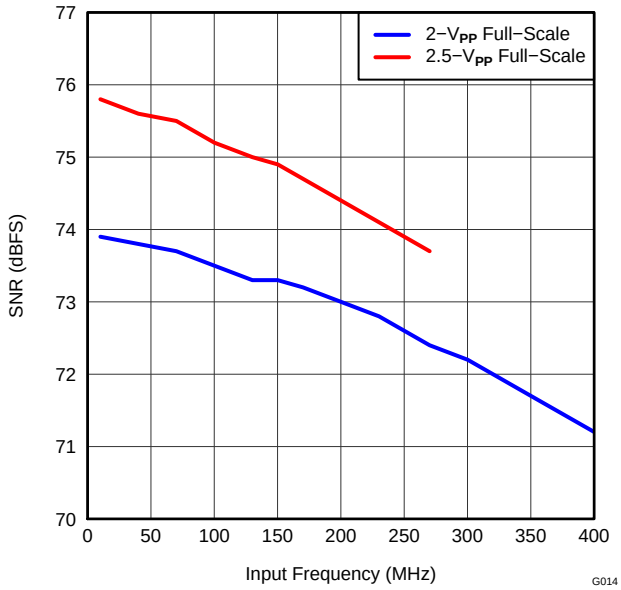


Figure 24. SNR vs INPUT FREQUENCY

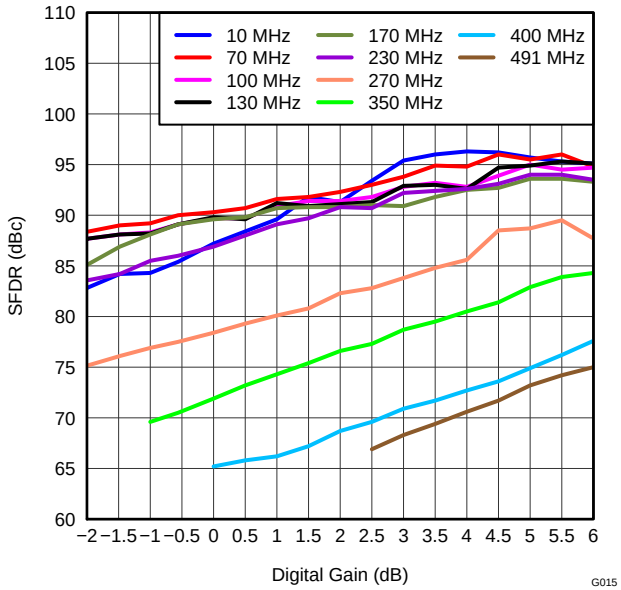


Figure 25. SFDR vs DIGITAL GAIN

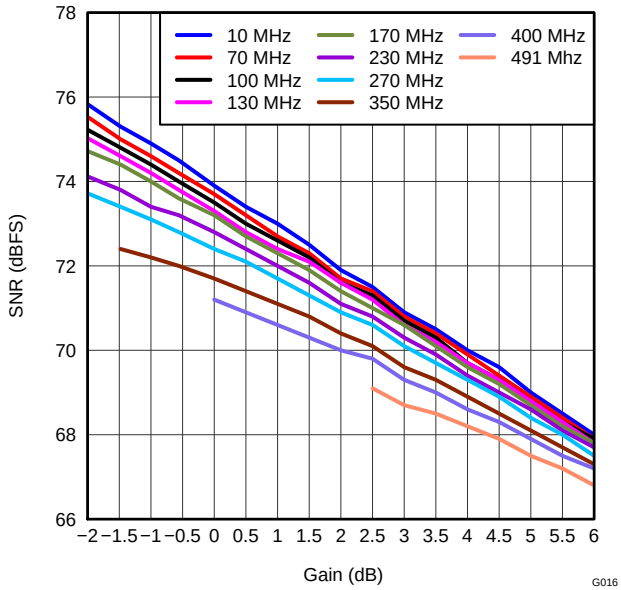


Figure 26. SNR vs DIGITAL GAIN

TYPICAL CHARACTERISTICS: ADS42LB69 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, QDR interface, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

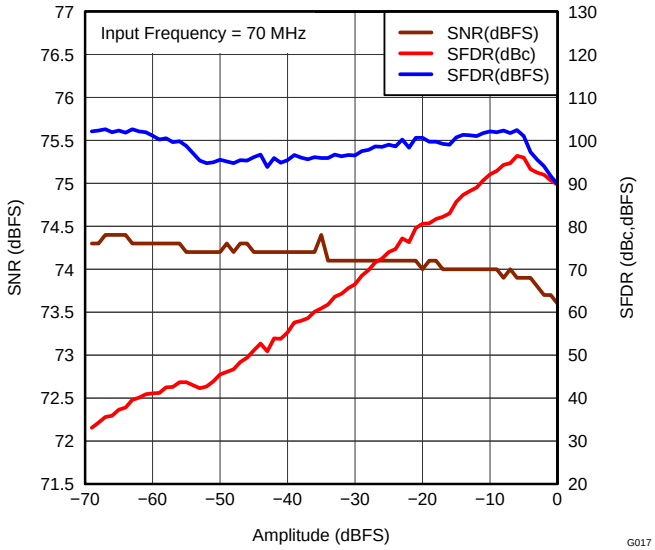


Figure 27. PERFORMANCE ACROSS INPUT AMPLITUDE (70 MHz)

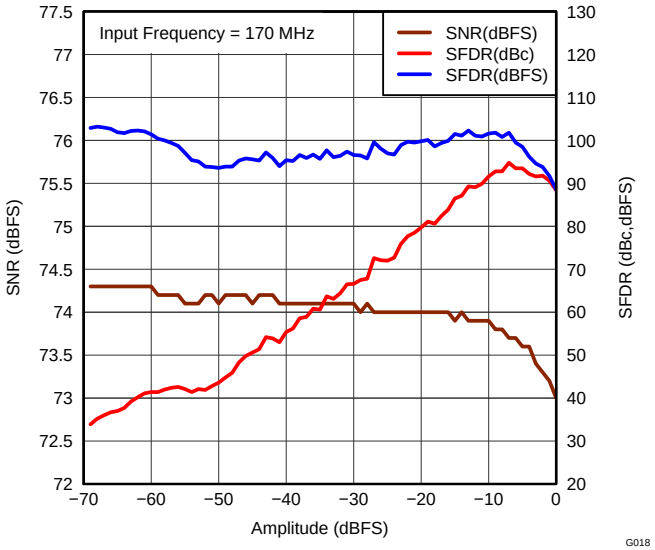


Figure 28. PERFORMANCE ACROSS INPUT AMPLITUDE (170 MHz)

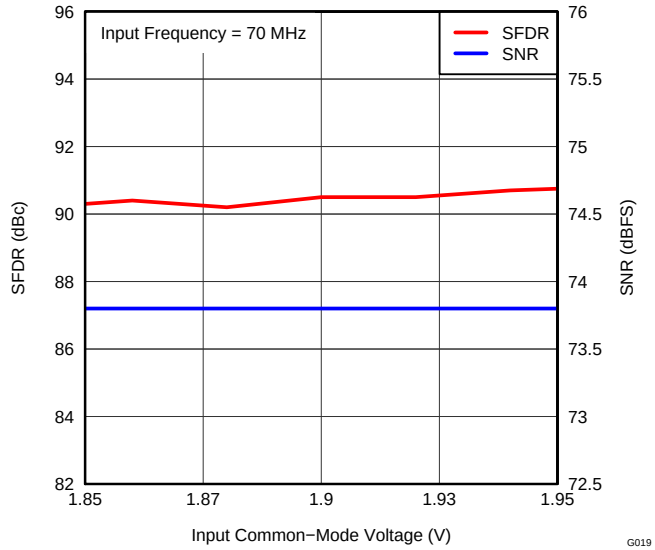


Figure 29. PERFORMANCE vs INPUT COMMON-MODE VOLTAGE (70 MHz)

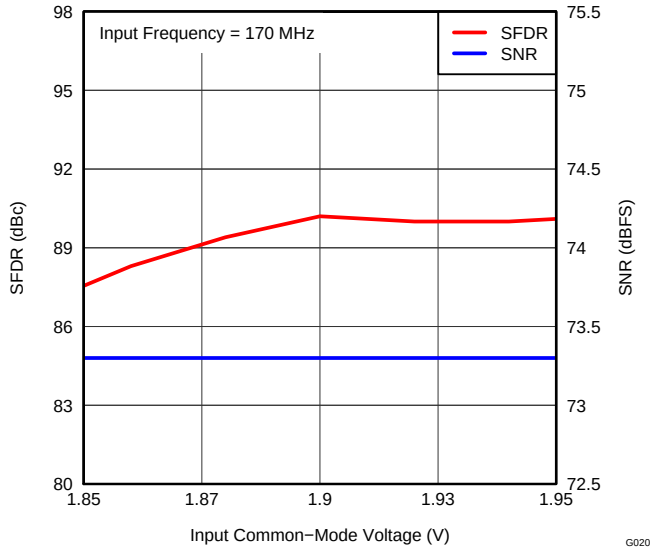


Figure 30. PERFORMANCE vs INPUT COMMON-MODE VOLTAGE (170 MHz)

TYPICAL CHARACTERISTICS: ADS42LB69 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, QDR interface, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

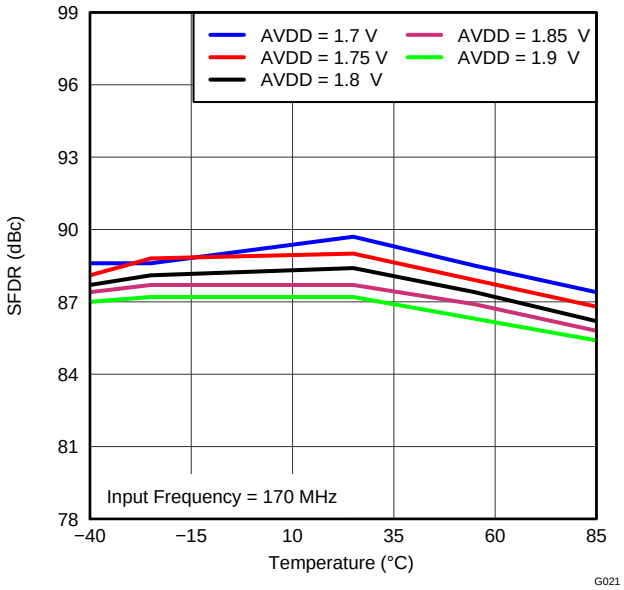


Figure 31. SFDR vs AVDD SUPPLY AND TEMPERATURE (170 MHz)

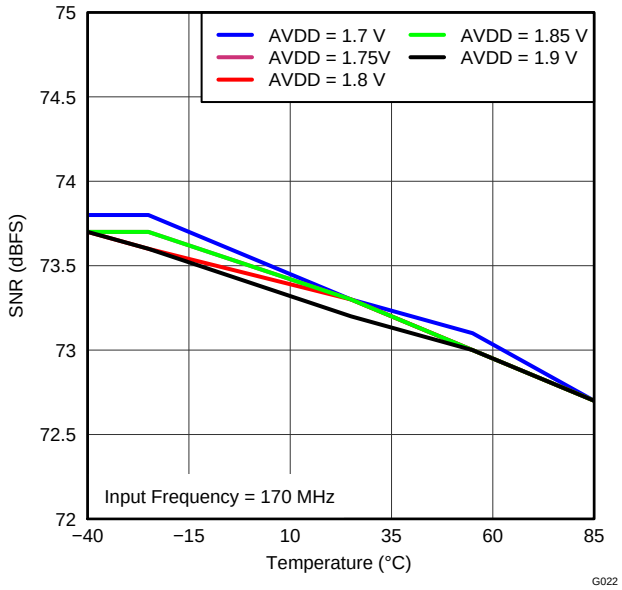


Figure 32. SNR vs AVDD SUPPLY AND TEMPERATURE (170 MHz)

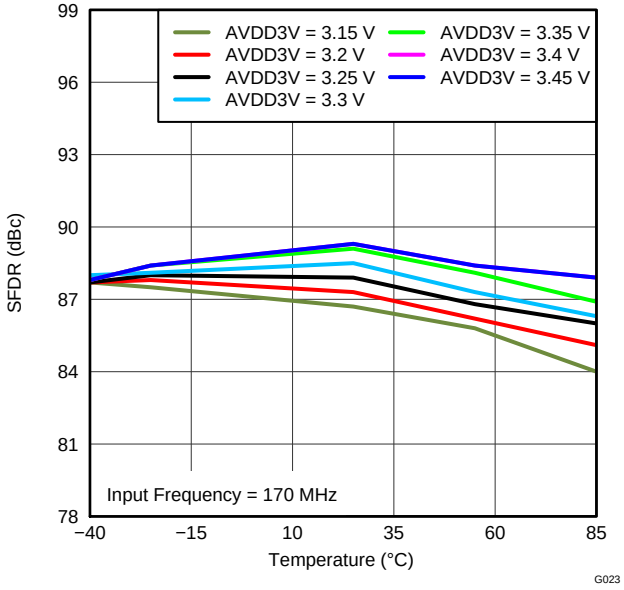


Figure 33. SFDR vs AVDD_BUF SUPPLY AND TEMPERATURE (170 MHz)

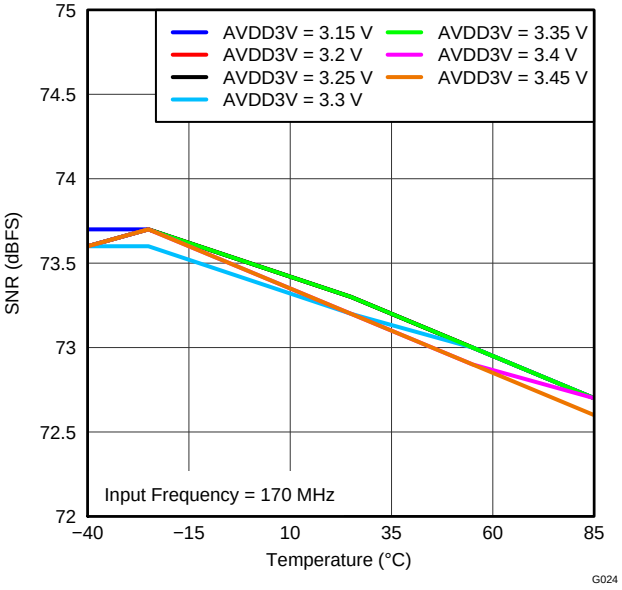


Figure 34. SNR vs AVDD_BUF SUPPLY AND TEMPERATURE (170 MHz)

TYPICAL CHARACTERISTICS: ADS42LB69 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, QDR interface, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

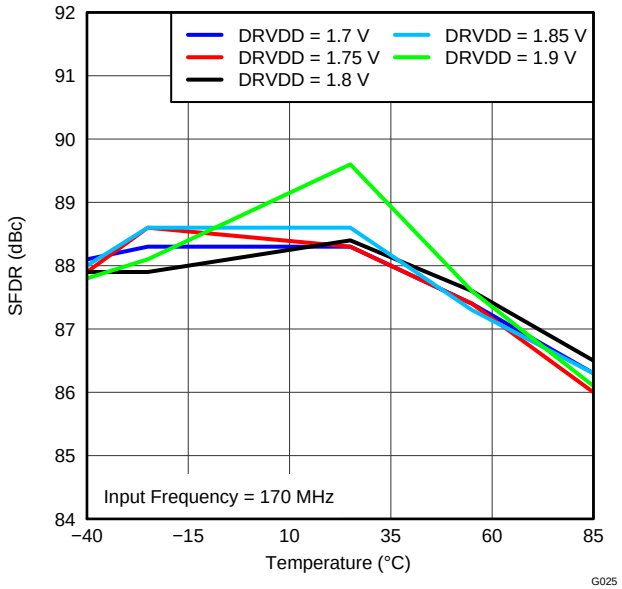


Figure 35. SFDR vs DRVDD SUPPLY AND TEMPERATURE (170 MHz)

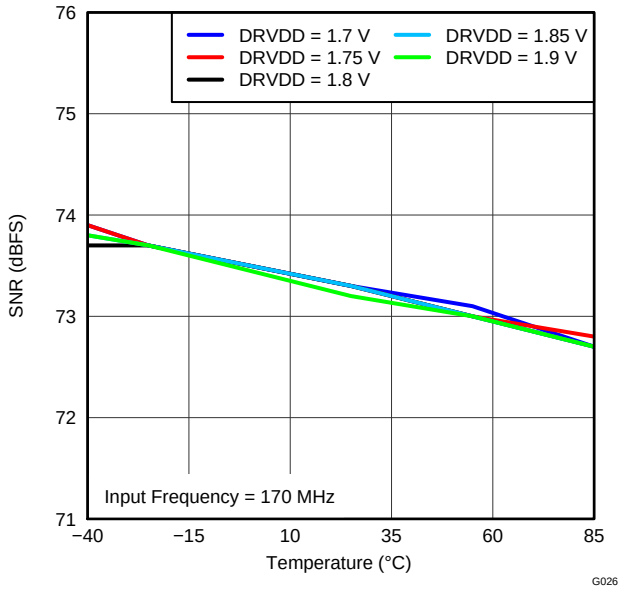


Figure 36. SNR vs DRVDD SUPPLY AND TEMPERATURE (170 MHz)

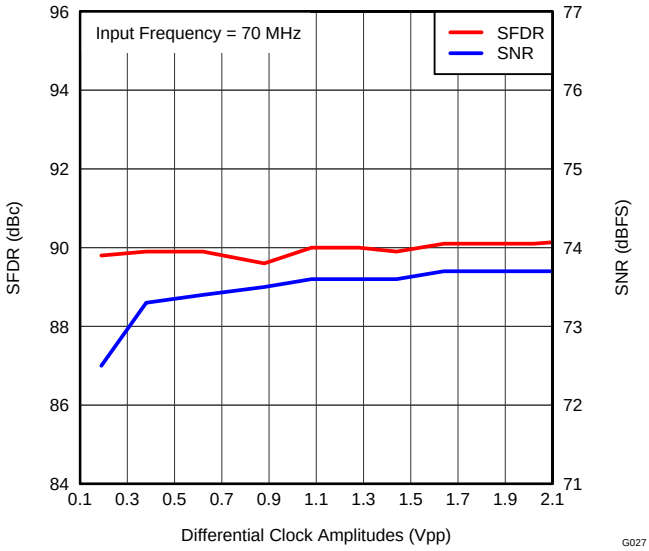


Figure 37. PERFORMANCE vs CLOCK AMPLITUDE (70 MHz)

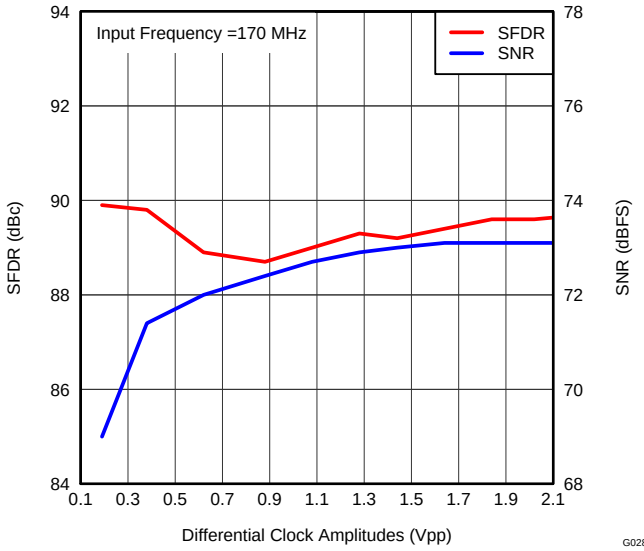


Figure 38. PERFORMANCE vs CLOCK AMPLITUDE (170 MHz)

TYPICAL CHARACTERISTICS: ADS42LB69 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, QDR interface, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

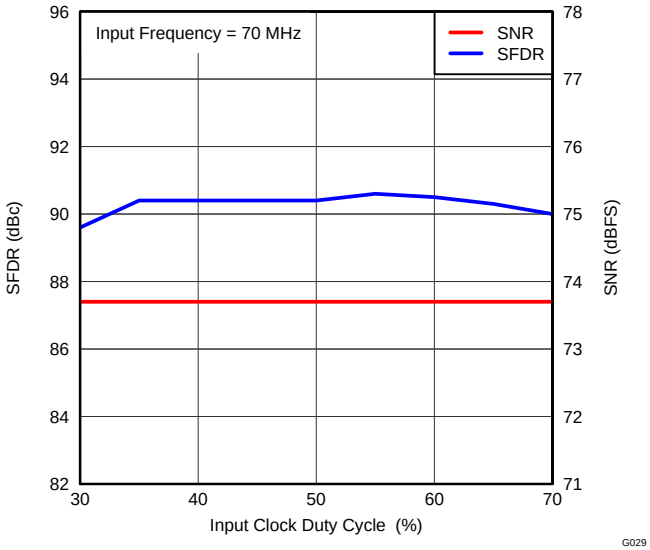


Figure 39. PERFORMANCE vs CLOCK DUTY CYCLE (70 MHz)

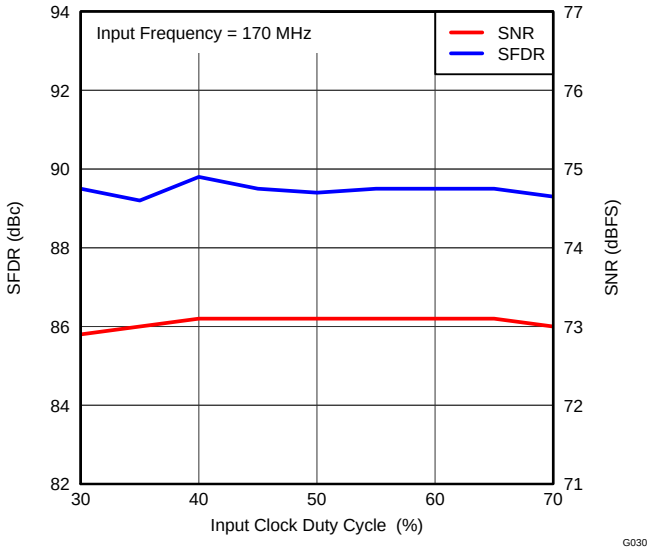


Figure 40. PERFORMANCE vs CLOCK DUTY CYCLE (170 MHz)

TYPICAL CHARACTERISTICS: ADS42LB49

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

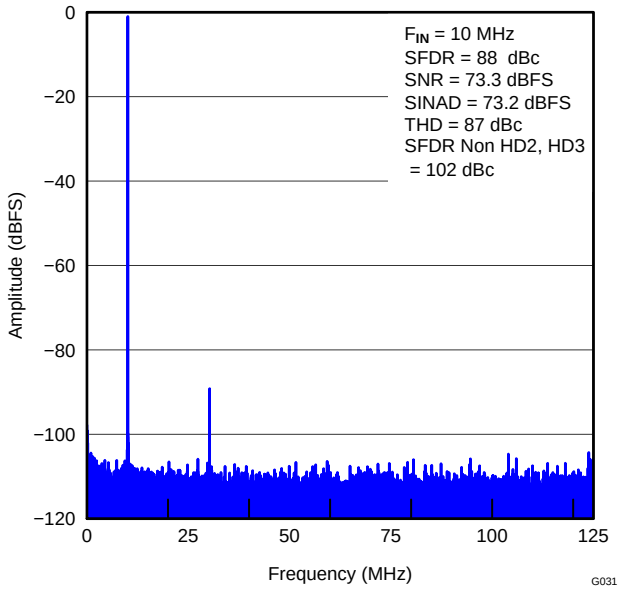


Figure 41. FFT FOR 10-MHz INPUT SIGNAL

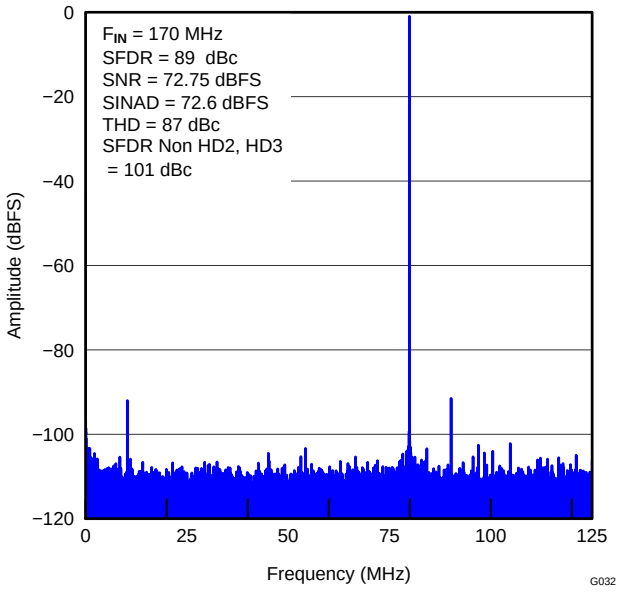


Figure 42. FFT FOR 170-MHz INPUT SIGNAL

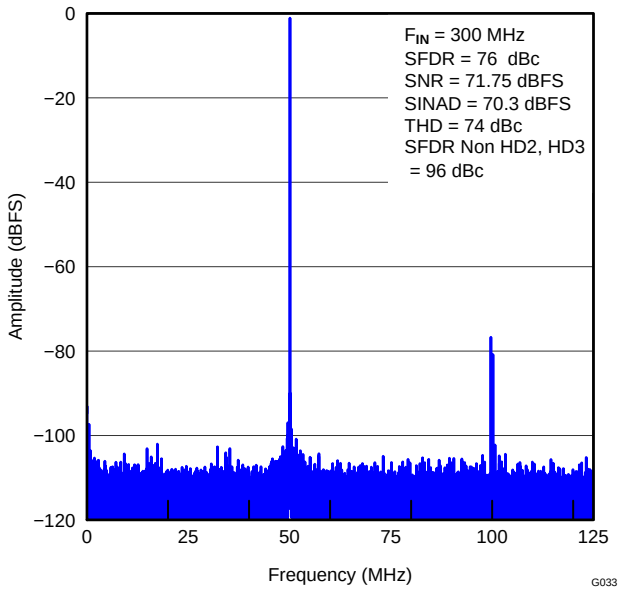


Figure 43. FFT FOR 300-MHz INPUT SIGNAL

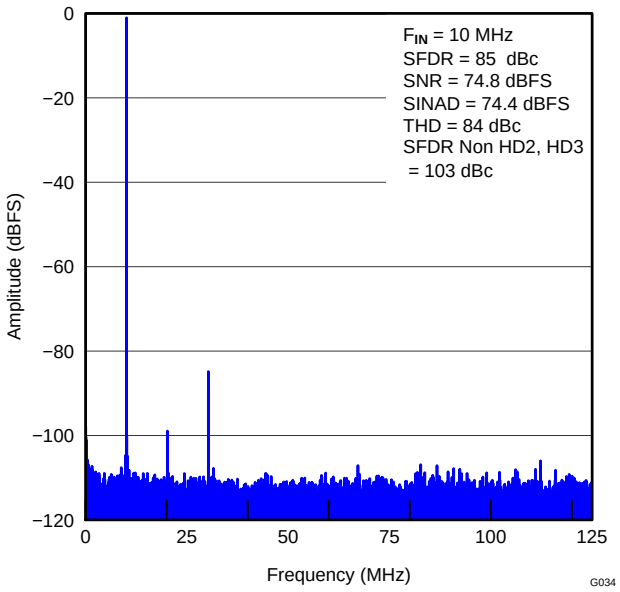


Figure 44. FFT FOR 10-MHz INPUT SIGNAL (2.5-V_{PP} Full-Scale)

TYPICAL CHARACTERISTICS: ADS42LB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

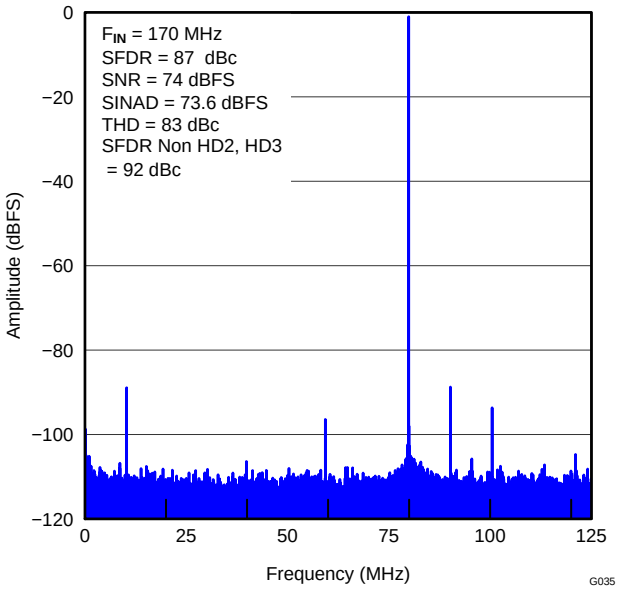


Figure 45. FFT FOR 170-MHz INPUT SIGNAL (2.5-V_{PP} Full-Scale)

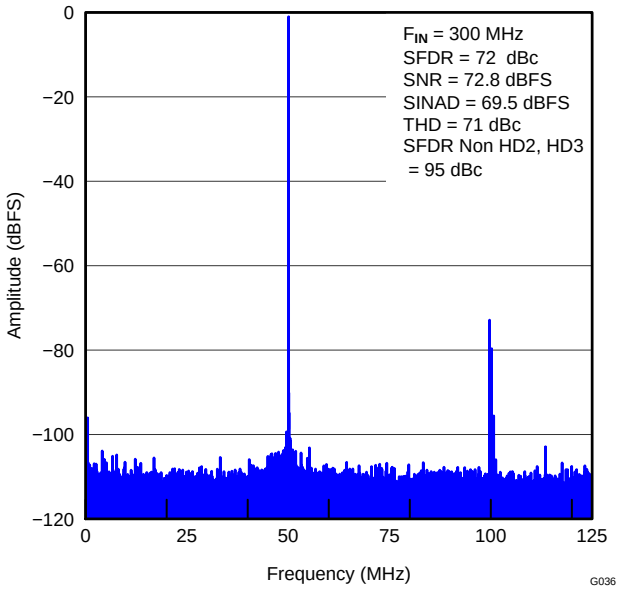


Figure 46. FFT FOR 300-MHz INPUT SIGNAL (2.5-V_{PP} Full-Scale)

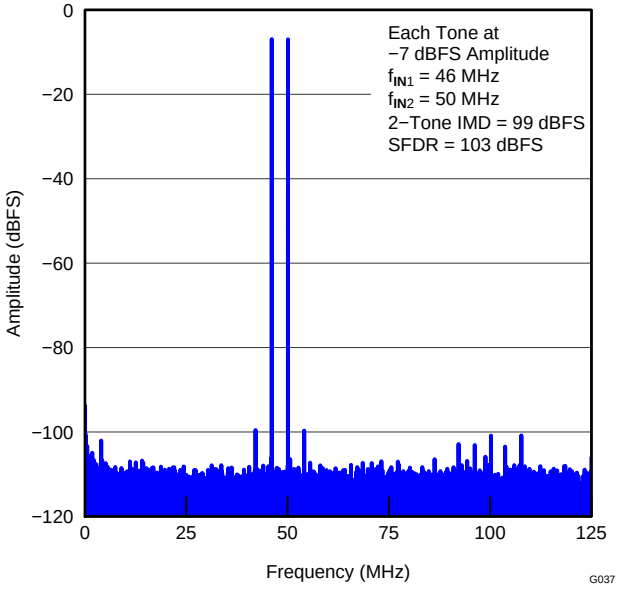


Figure 47. FFT FOR TWO-TONE INPUT SIGNAL (At –7 dBFS, 46 MHz and 50 MHz)

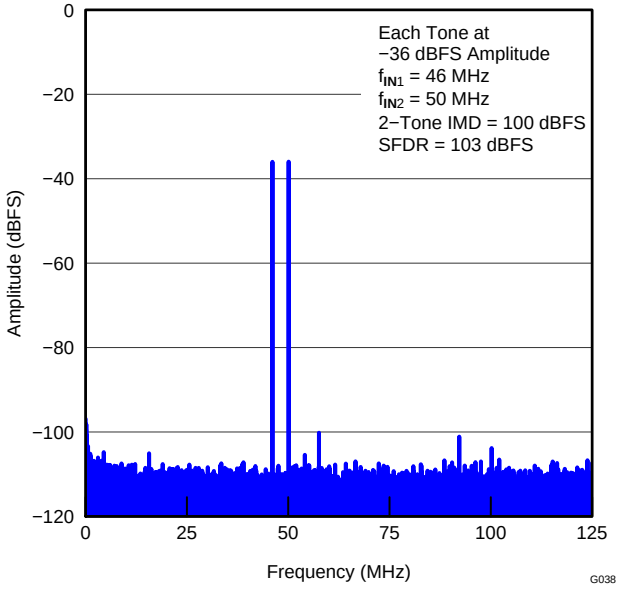


Figure 48. FFT FOR TWO-TONE INPUT SIGNAL (At –36 dBFS, 46 MHz and 50 MHz)

TYPICAL CHARACTERISTICS: ADS42LB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

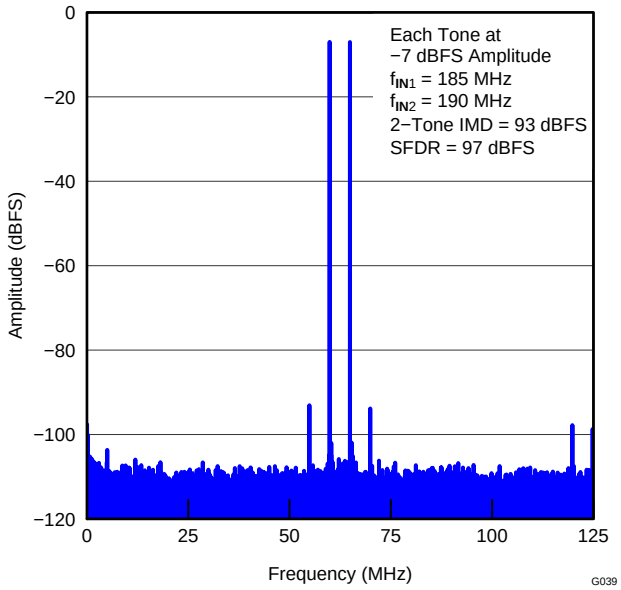


Figure 49. FFT FOR TWO-TONE INPUT SIGNAL (At –7 dBFS, 185 MHz and 190 MHz)

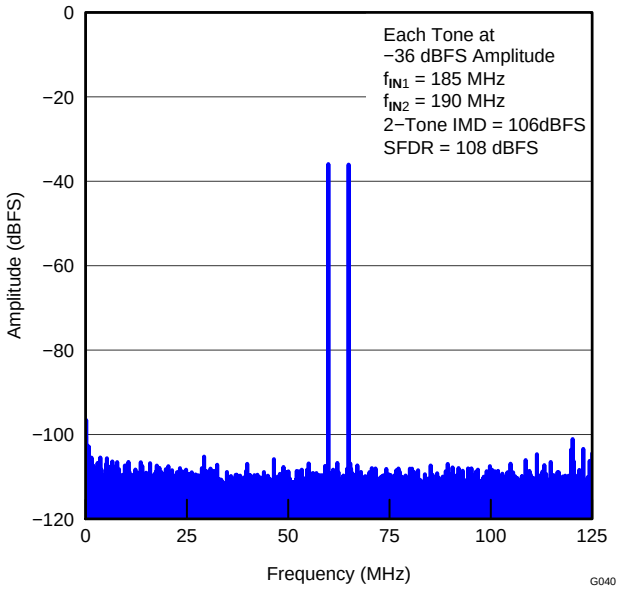


Figure 50. FFT FOR TWO-TONE INPUT SIGNAL (At –36 dBFS, 185 MHz and 190 MHz)

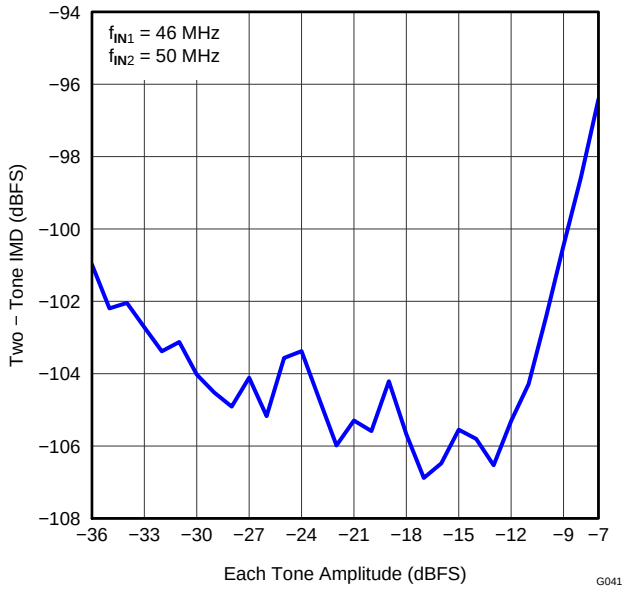


Figure 51. IMD3 vs INPUT AMPLITUDE (46 MHz and 50 MHz)

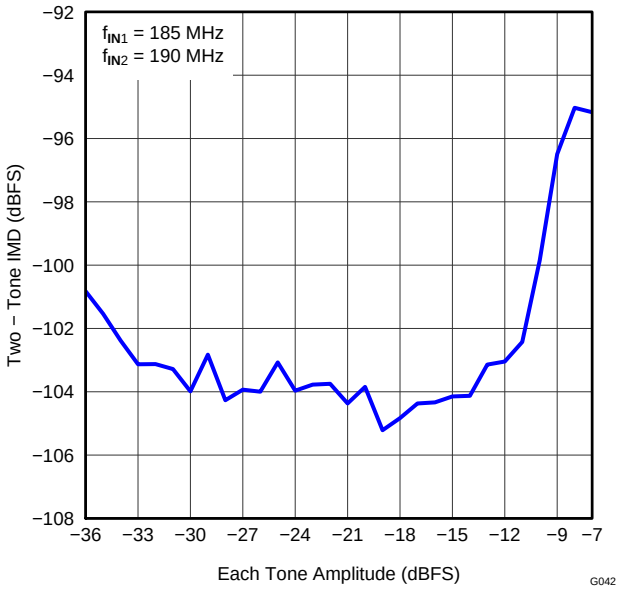


Figure 52. IMD3 vs INPUT AMPLITUDE (185 MHz and 190 MHz)

TYPICAL CHARACTERISTICS: ADS42LB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

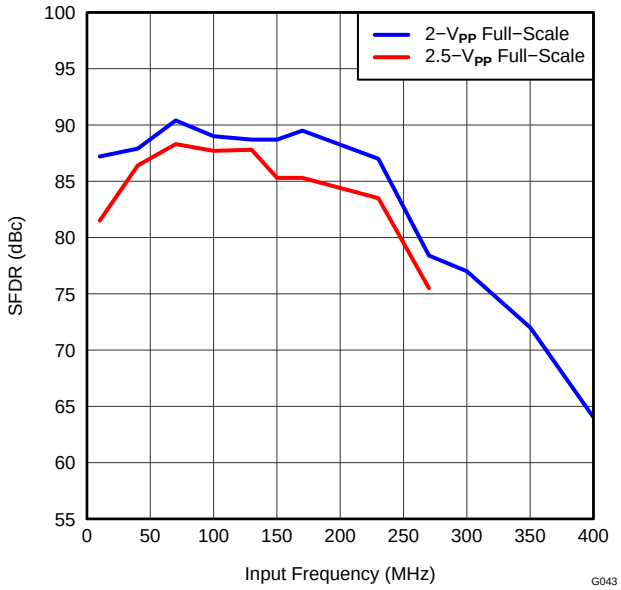


Figure 53. SFDR vs INPUT FREQUENCY

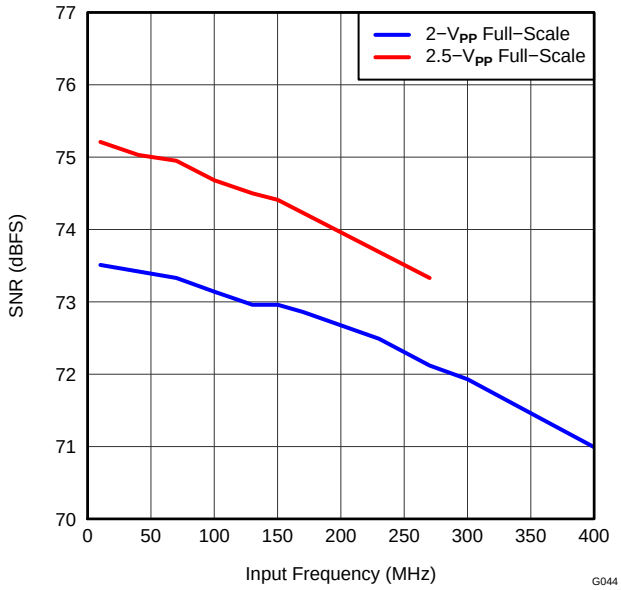


Figure 54. SNR vs INPUT FREQUENCY

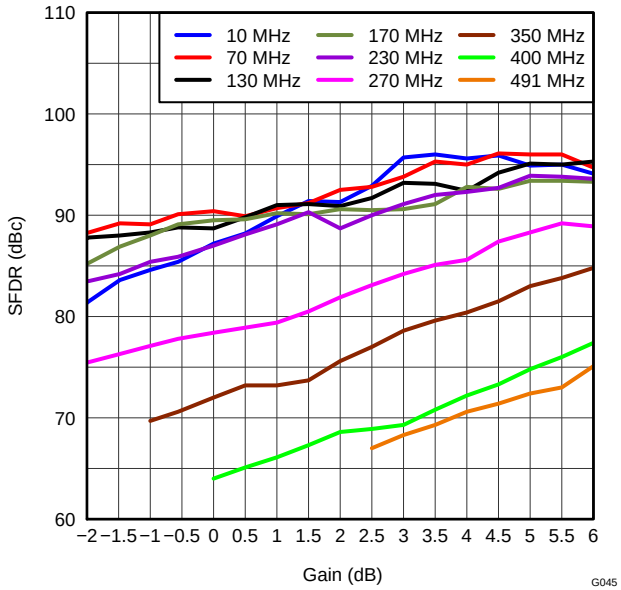


Figure 55. SFDR vs DIGITAL GAIN

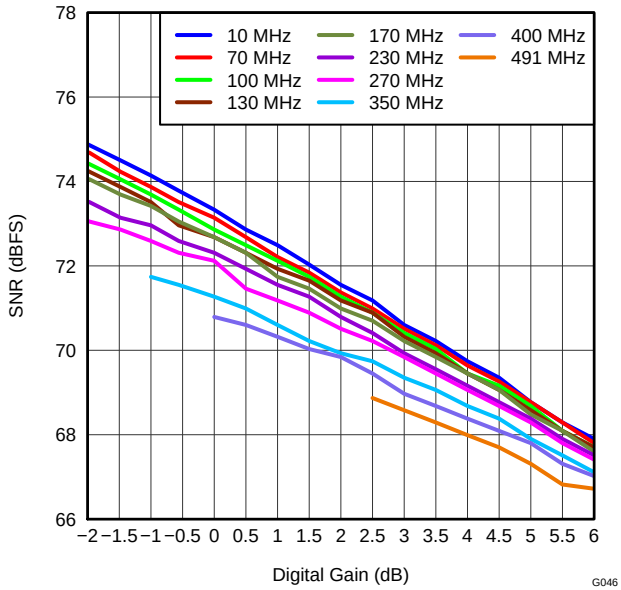


Figure 56. SNR vs DIGITAL GAIN

TYPICAL CHARACTERISTICS: ADS42LB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

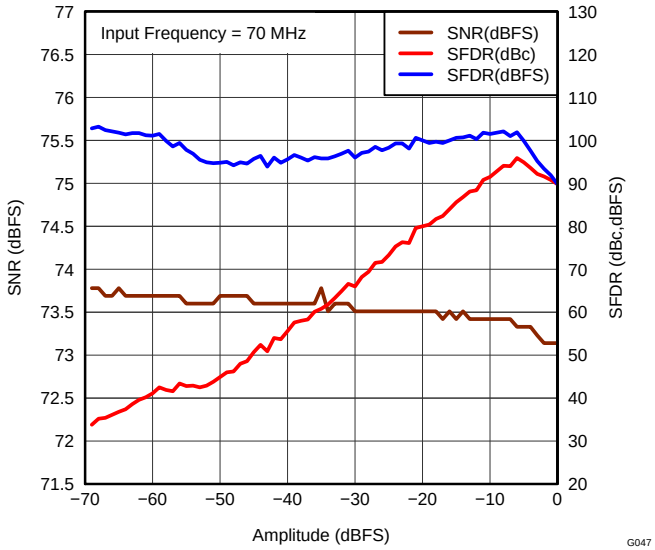


Figure 57. PERFORMANCE ACROSS INPUT AMPLITUDE (70 MHz)

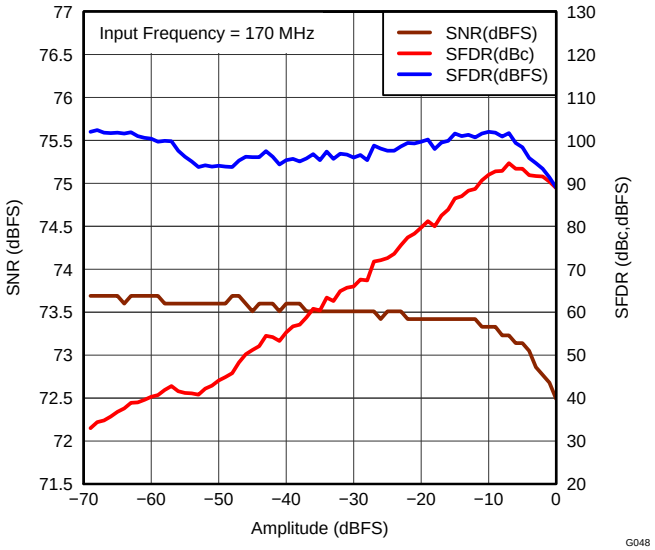


Figure 58. PERFORMANCE ACROSS INPUT AMPLITUDE (170 MHz)

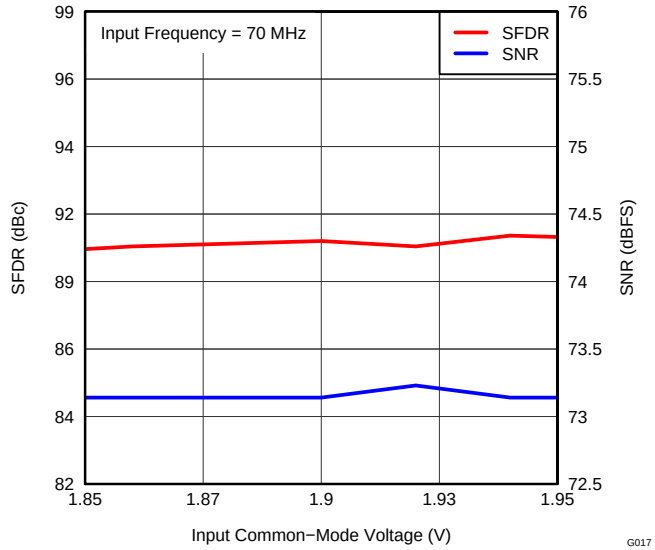


Figure 59. PERFORMANCE vs INPUT COMMON-MODE VOLTAGE (70 MHz)

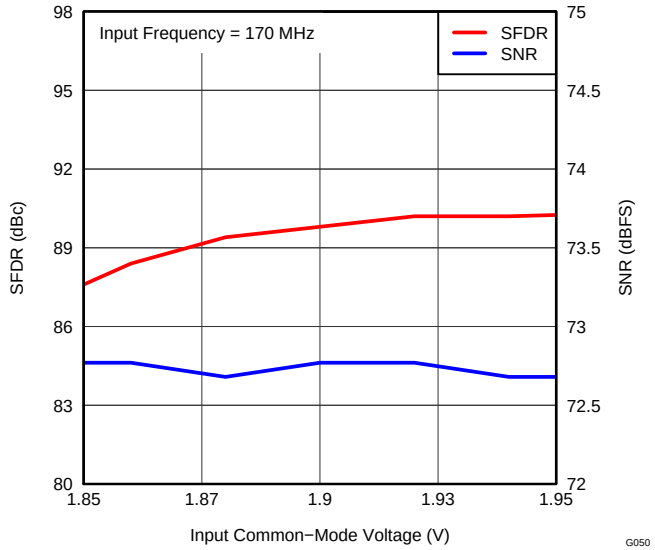


Figure 60. PERFORMANCE vs INPUT COMMON-MODE VOLTAGE (170 MHz)

TYPICAL CHARACTERISTICS: ADS42LB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

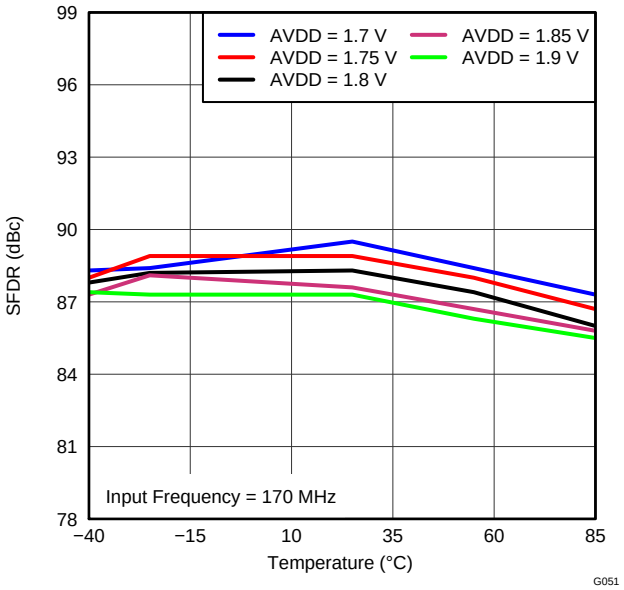


Figure 61. SFDR vs AVDD SUPPLY AND TEMPERATURE (170 MHz)

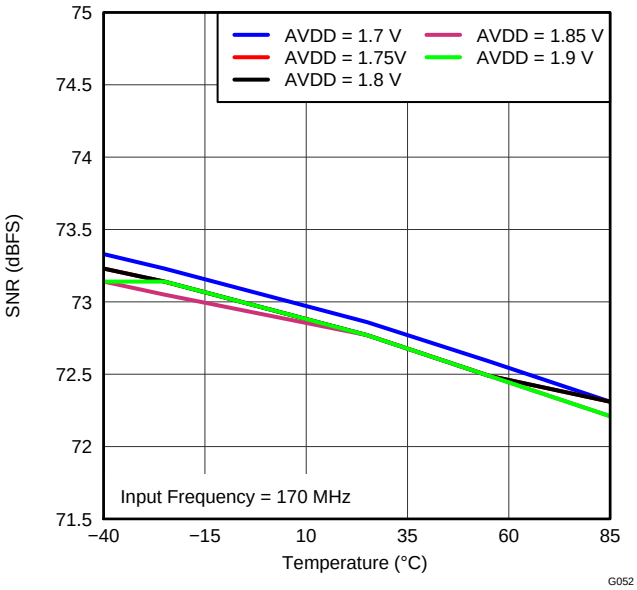


Figure 62. SNR vs AVDD SUPPLY AND TEMPERATURE (170 MHz)

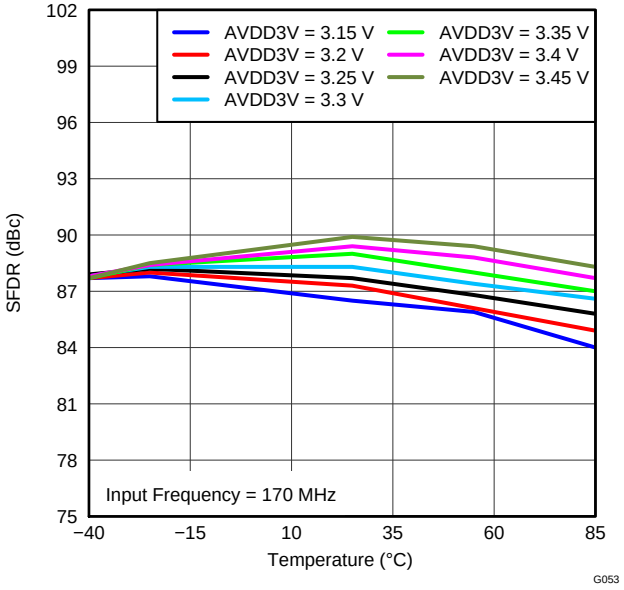


Figure 63. SFDR vs AVDD_BUF SUPPLY AND TEMPERATURE (170 MHz)

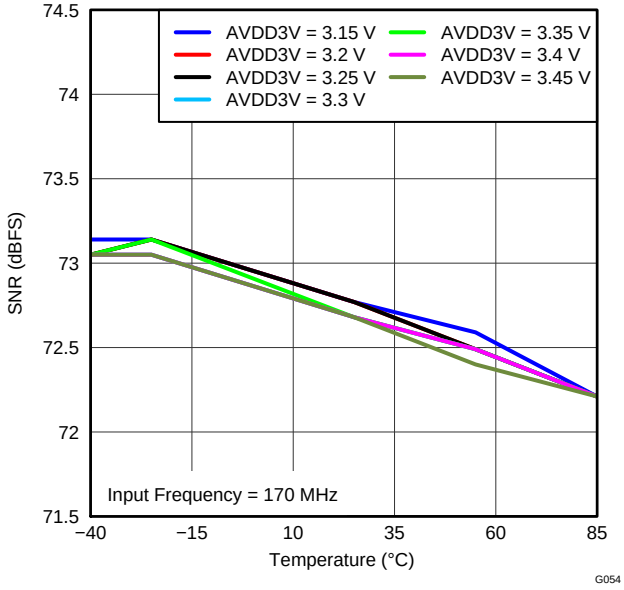


Figure 64. SNR vs AVDD_BUF SUPPLY AND TEMPERATURE (170 MHz)

TYPICAL CHARACTERISTICS: ADS42LB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

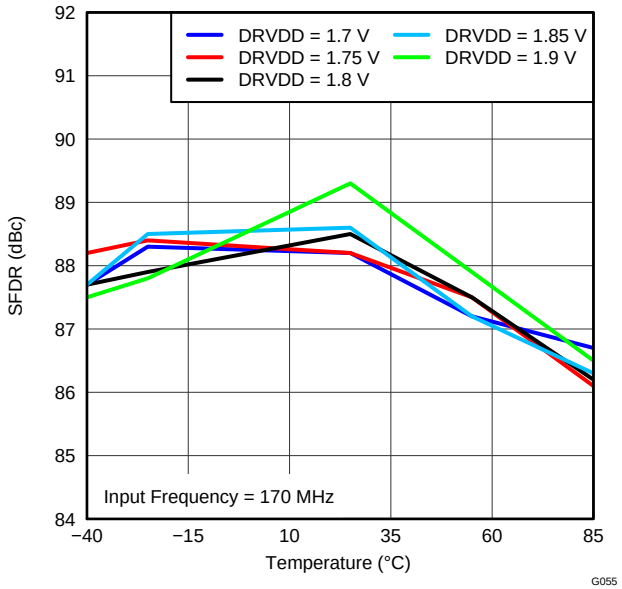


Figure 65. SFDR vs DRVDD SUPPLY AND TEMPERATURE (170 MHz)

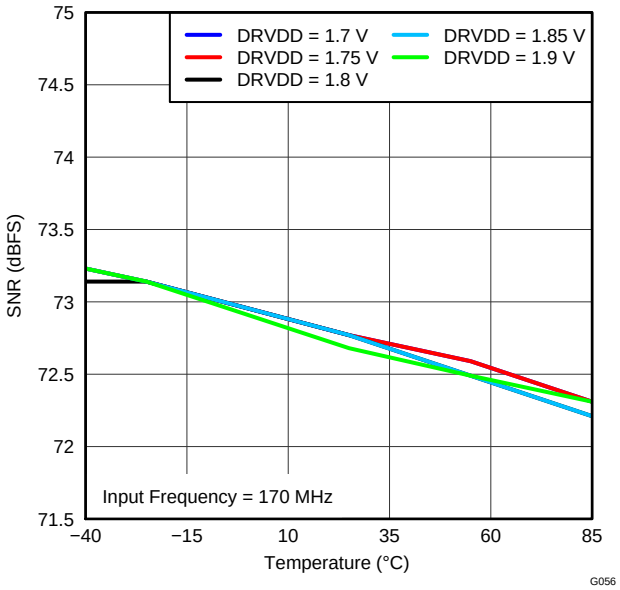


Figure 66. SNR vs DRVDD SUPPLY AND TEMPERATURE (170 MHz)

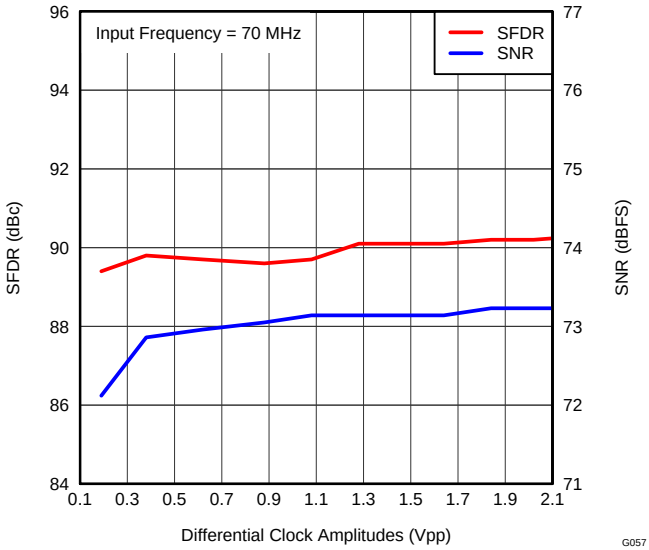


Figure 67. PERFORMANCE vs CLOCK AMPLITUDE (70 MHz)

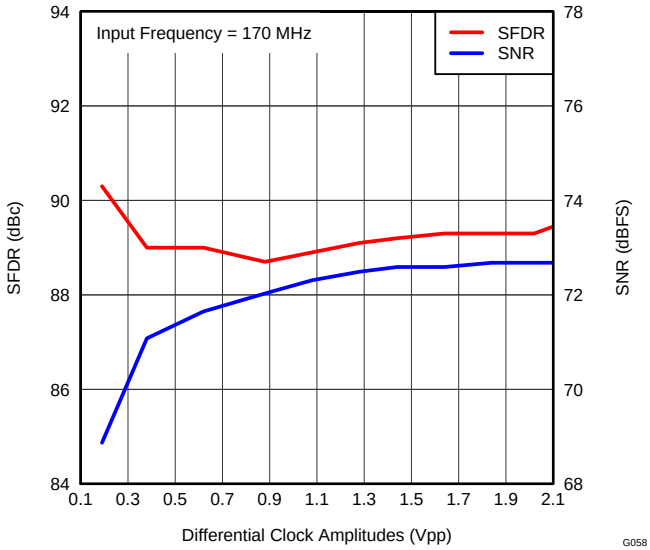


Figure 68. PERFORMANCE vs CLOCK AMPLITUDE (170 MHz)

TYPICAL CHARACTERISTICS: ADS42LB49 (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

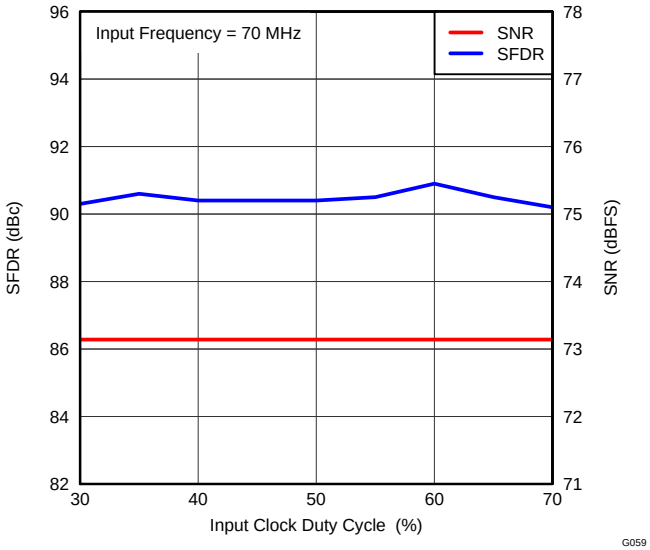


Figure 69. PERFORMANCE vs CLOCK DUTY CYCLE (70 MHz)

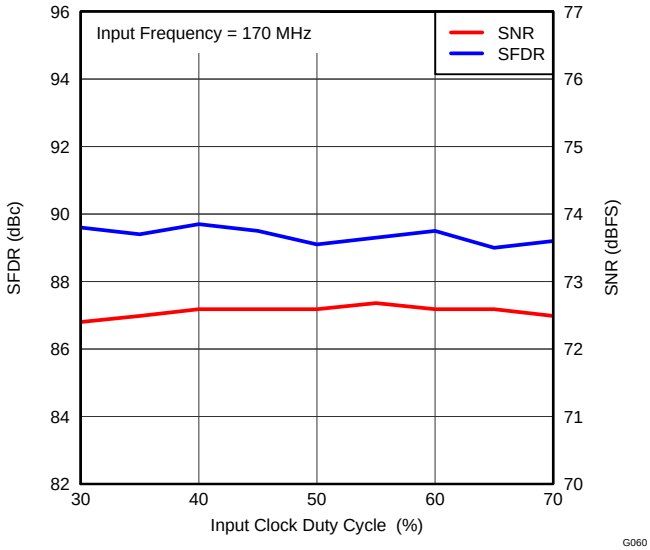


Figure 70. PERFORMANCE vs CLOCK DUTY CYCLE (170 MHz)

TYPICAL CHARACTERISTICS: Common

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

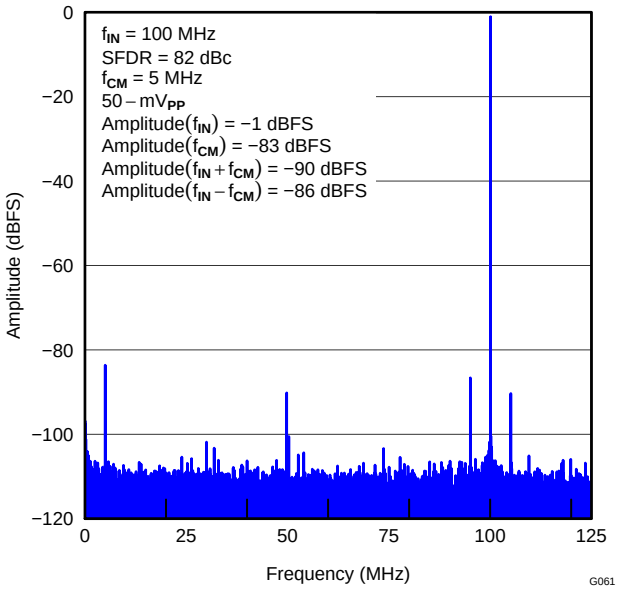


Figure 71. CMRR FFT

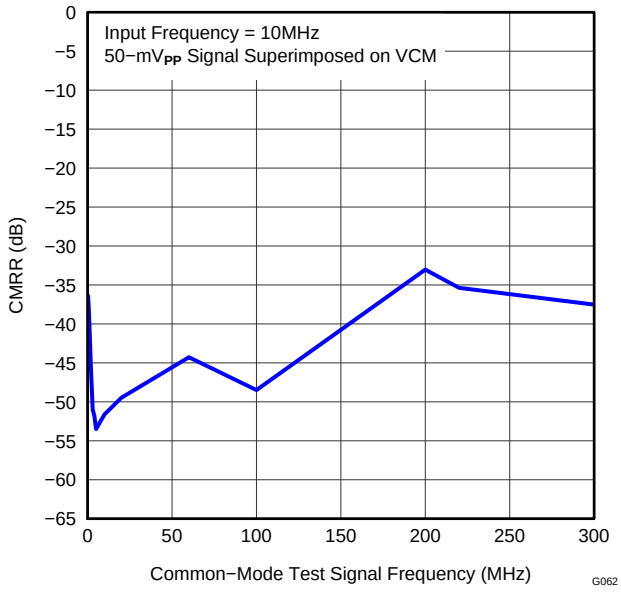


Figure 72. CMRR vs TEST SIGNAL FREQUENCY

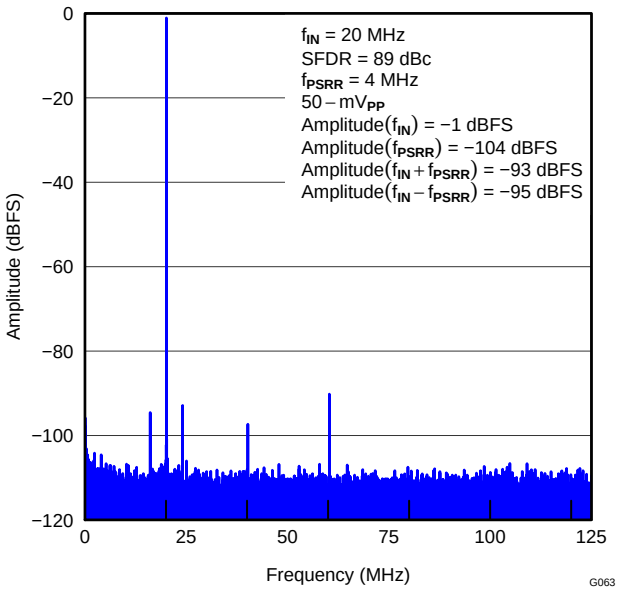


Figure 73. PSRR FFT FOR AVDD SUPPLY

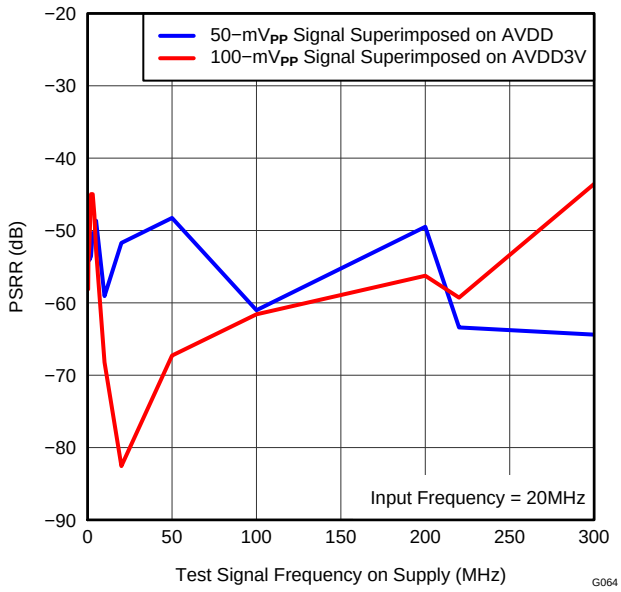


Figure 74. PSRR vs TEST SIGNAL FREQUENCY

TYPICAL CHARACTERISTICS: Common (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 32k-point FFT, unless otherwise noted.

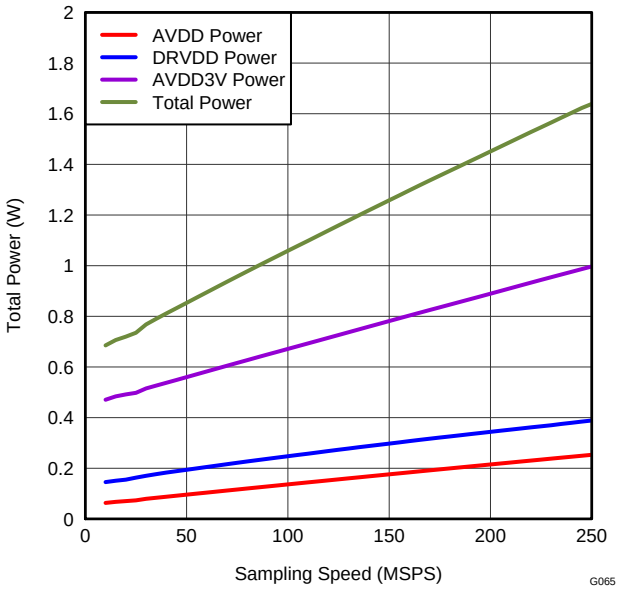


Figure 75. TOTAL POWER vs SAMPLING FREQUENCY

TYPICAL CHARACTERISTICS: Contour

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 65k-point FFT, unless otherwise noted.

Spurious-Free Dynamic Range (SFDR): General

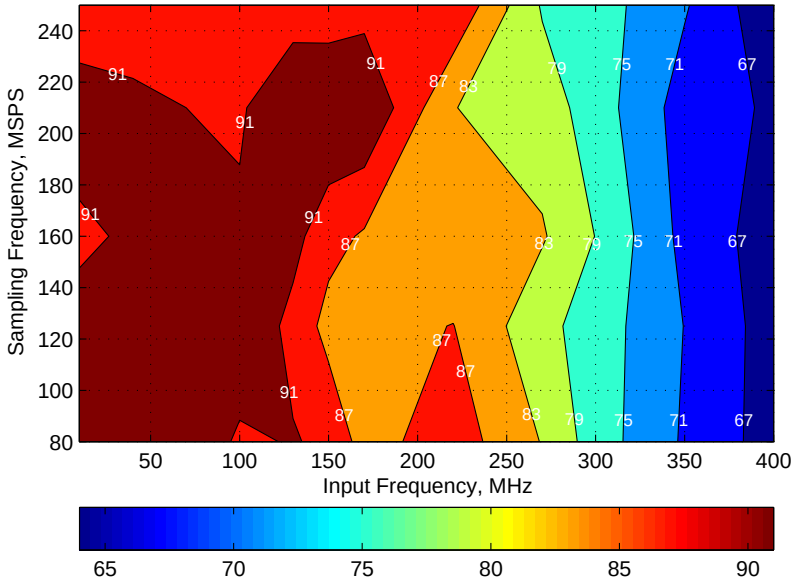


Figure 76. SFDR (0-dB Gain)

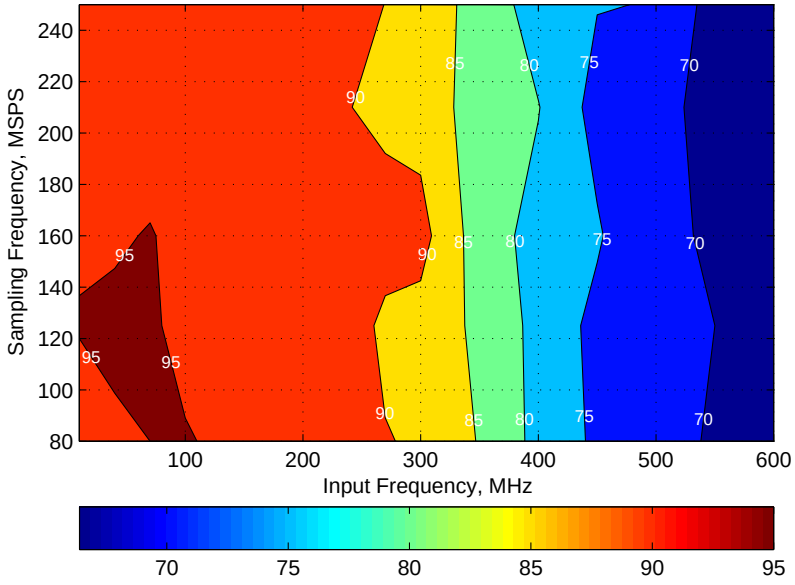


Figure 77. SFDR (6-dB Gain)

TYPICAL CHARACTERISTICS: Contour (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 65k-point FFT, unless otherwise noted.

Signal-to-Noise Ratio (SNR): ADS42LB69

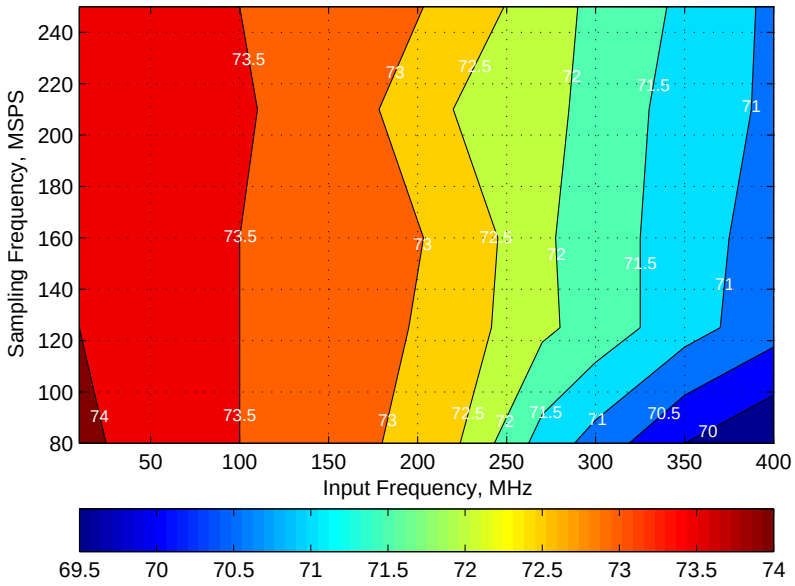


Figure 78. SNR (0-dB Gain, 16 Bits)

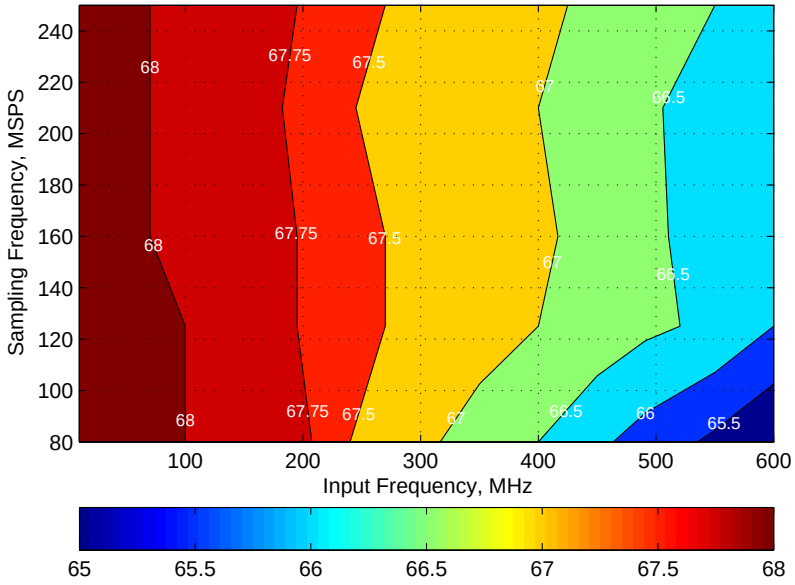


Figure 79. SNR (6-dB Gain, 16 Bits)

TYPICAL CHARACTERISTICS: Contour (continued)

Typical values are at T_A = +25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = +85°C, ADC sampling rate = 250 MSPS, 50% clock duty cycle, AVDD3V = 3.3 V, AVDD = DRVDD = 1.8 V, –1-dBFS differential input, and 65k-point FFT, unless otherwise noted.

Signal-to-Noise Ratio (SNR): ADS42LB49

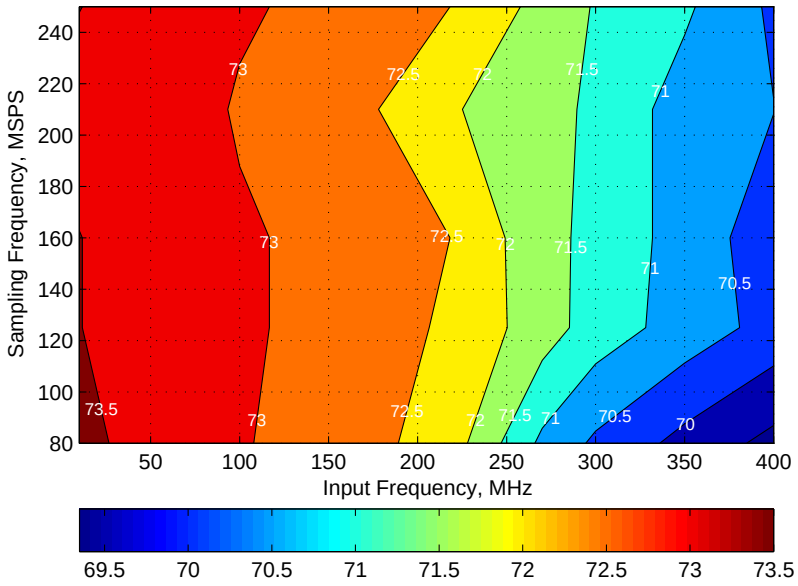


Figure 80. SNR (0-dB Gain, 14 Bits)

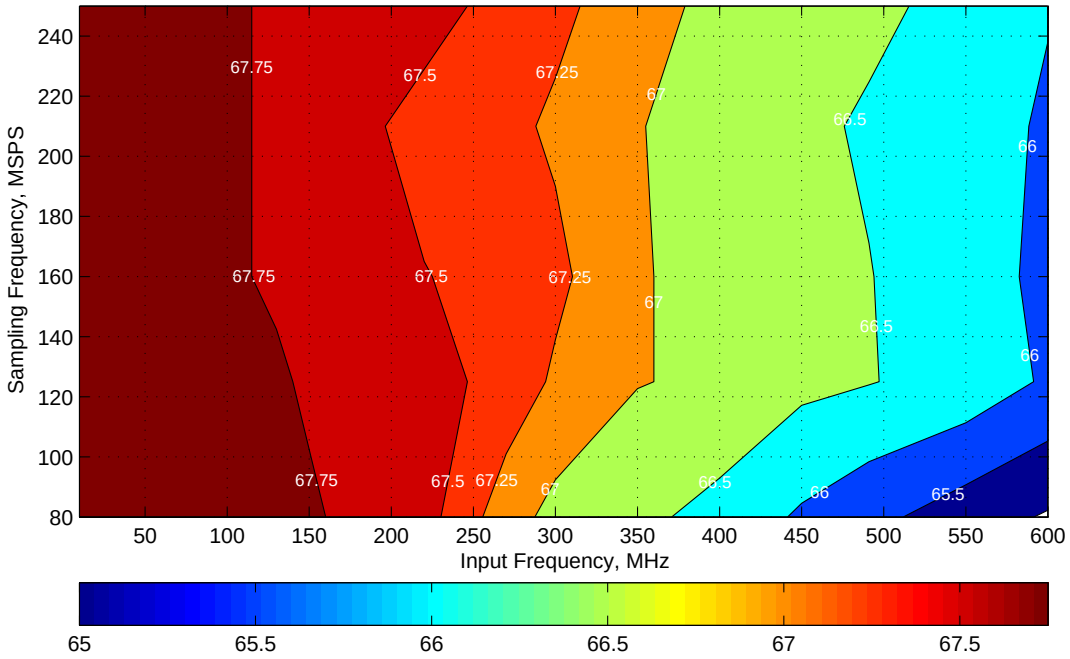


Figure 81. SNR (6-dB Gain, 14 Bits)

DEVICE CONFIGURATION

The ADS42LB49 and ADS42LB69 can be configured using a serial programming interface, as described in this section. In addition, the device has two bidirectional parallel pins (CTRL1 and CTRL2). By default, these pins act as input pins and control the power-down modes, as described in Table 5 and Table 6. These pins can be programmed as output pins that deliver overrange information by setting the PDN/OVR_FOR_CTRL_PINS register bit.

Table 5. PDN/OVR_FOR_CTRL_PINS Bit (Set to '0')

CTRL2	CTRL1	PIN DIRECTION	FUNCTION
Low	Low	Input	Default operation
Low	High	Input	Channel A power-down
High	Low	Input	Channel B powers down in QDR mode. Do not use in DDR mode.
High	High	Input	Channels A and B power-down

Table 6. PDN/OVR_FOR_CTRL_PINS Bit (Set to '1')

CTRL2	CTRL1	PIN DIRECTION
Carries OVR for channel B	Carries OVR for channel A	Output

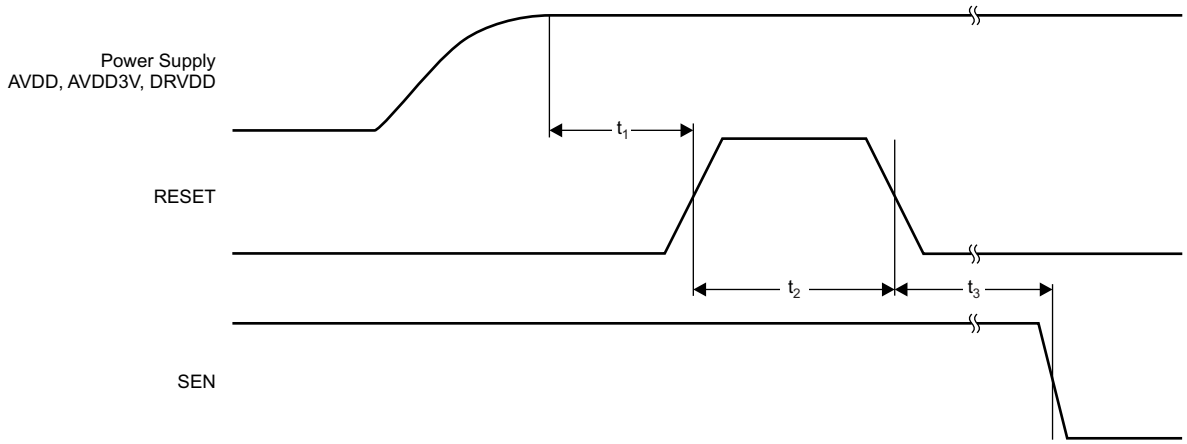
DETAILS OF SERIAL INTERFACE

The ADC has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data) and SDOUT (serial interface data output) pins. Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK rising edge when SEN is active (low). The serial data are loaded into the register at every 16th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active SEN pulse. The interface can work with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers must be initialized to their default values through a *hardware reset* by applying a high pulse on the RESET pin (of widths greater than 10 ns), as shown in Figure 82 and Table 7. If required, serial interface registers can later be cleared during operation by:

1. Either through a hardware reset or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 08h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.



NOTE: After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin.

Figure 82. Reset Timing Diagram

Table 7. Reset Timing (1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from AVDD and DRVDD power-up to active RESET pulse	1			ms
t_2	Reset pulse width	Active RESET signal pulse width	10			ns
					1	µs
t_3	Register write delay	Delay from RESET disable to SEN active	100			ns

(1) Typical values at +25°C; minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, unless otherwise noted.

Serial Register Write

The internal register of the ADS42LB49 and ADS42LB69 can be programmed following these steps:

1. Drive SEN pin low
2. Set the R/W bit to '0' (bit A7 of the 8 bit address)
3. Set bit A6 in the address field to '0'
4. Initiate a serial interface cycle specifying the address of the register (A5 to A0) whose content must be written
5. Write 8 bit data which is latched in on the rising edge of SCLK.

Figure 83 and Table 8 illustrate these steps.

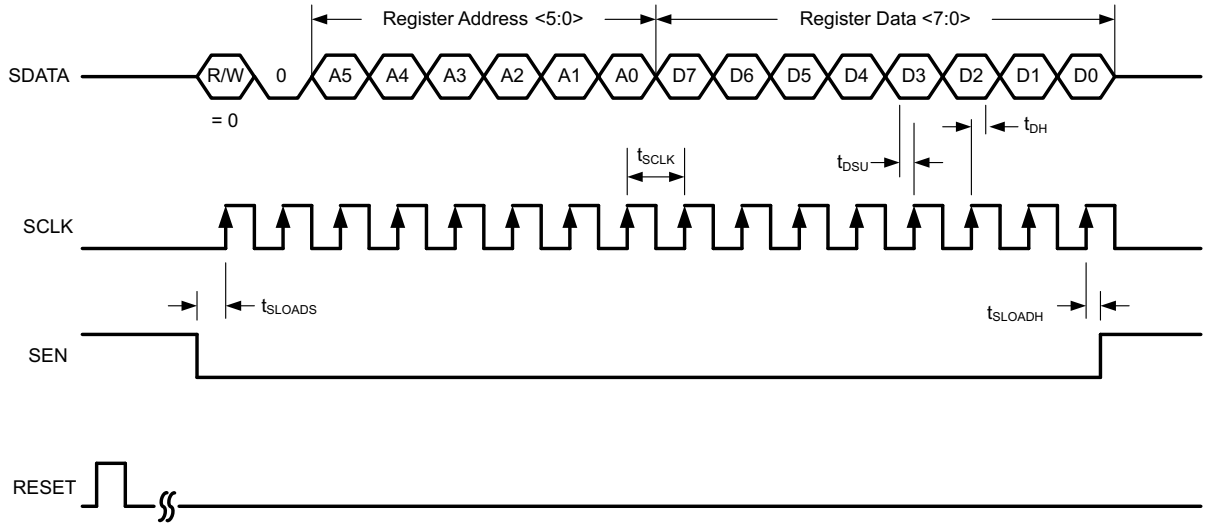


Figure 83. Serial Register Write Timing Diagram

Table 8. Serial Interface Timing (only when Serial Interface is Used)(1)

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	> dc		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDIO setup time	25			ns
t_{DH}	SDIO hold time	25			ns

(1) Typical values are at +25°C; minimum and maximum values across the full temperature range: T_{MIN} = –40°C to T_{MAX} = +85°C, AVDD3V = 3.3 V, and AVDD = DRVDD = 1.8 V, unless otherwise noted.

Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back using the SDOUT pin. This read-back mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC.

1. Drive SEN pin low
2. Set the R/W bit (A7) to '1'. This setting disables any further writes to the registers
3. Set bit A6 in the address field to 0.
4. Initiate a serial interface cycle specifying the address of the register (A5 to A0) whose content has to be read.
5. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin.
6. The external controller can latch the contents at the SCLK falling edge.
7. To enable register writes, reset the R/W register bit to '0'.

Figure 84 illustrates these steps. When READOUT is disabled, the SDOUT pin is in a high-impedance mode. If serial readout is not used, the SDOUT pin must float.

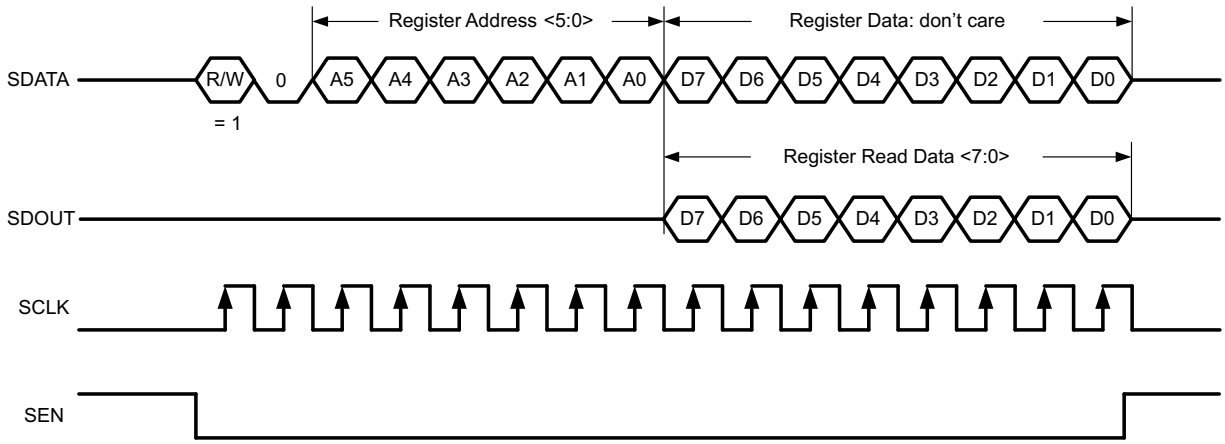


Figure 84. Serial Register Readout Timing Diagram

SUMMARY OF SERIAL INTERFACE REGISTERS

REGISTER ADDRESS	REGISTER DATA							
A7–A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
6	1	0	0	0	0	0	CLK DIV	
7	0	0	0	0	0	SYNCIN DELAY		
8	PDN CHA	PDN CHB	STDBY	DATA FORMAT	DIS CTRL PINS	TEST PAT ALIGN	0	RESET
B	CHA GAIN					CHA GAIN EN	0	FLIP DATA
C	CHBGAIN					CHB GAIN EN	OVR ON LSB	
D	0	1	1	0	1	1	0	FAST OVR ON PIN
F	CHA TEST PATTERNS				CHB TEST PATTERNS			
10	CUSTOM PATTERN 1 (15:8)							
11	CUSTOM PATTERN 1 (7:0)							
12	CUSTOM PATTERN 2 (15:8)							
13	CUSTOM PATTERN 2 (7:0)							
14	0	0	0	0	LVDS CLK STRENGTH	LVDS DATA STRENGTH	DISABLE OUTPUT CHA	DISABLE OUTPUT CHB
15	0	0	0	0	0	0	0	DDR - QDR
16	0	0	DDR OUTPUT TIMING					0
17	LVDS CLK STRENGTH EN	0	QDR TIMING CHA					INV CLK OUT CHA
18	0	0	QDR TIMING CHB					INV CLK OUT CHB
1F	Always write '0'	FAST OVR THRESHOLD						
20	0	0	0	0	0	0	0	PDN/OVR FOR CTRL PINS

DESCRIPTION OF SERIAL INTERFACE REGISTERS

REGISTER ADDRESS	REGISTER DATA							
A7-A0 IN HEX	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
6	1	0	0	0	0	0	CLK DIV	

Default: 80h

D[1:0]	**CLK DIV**	Internal clock divider for input sample clock
00	Divide-by-1 (clock divider bypassed)	
01	Divide-by-2	
10	Divide-by-1	
11	Divide-by-4	

REGISTER ADDRESS	REGISTER DATA							
A7-A0 IN HEX	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
7	0	0	0	0	0	SYNCIN DELAY		

Default: 00h

D[2:0] **SYNCIN DELAY** Controls the delay of the SYNCIN input with respect to the input clock. Typical values for the expected delay of different settings are:

000	0-ps delay	100	240-ps delay
001	60-ps delay	101	300-ps delay
010	120-ps delay	110	360-ps delay
011	180-ps delay	111	420-ps delay

REGISTER ADDRESS	REGISTER DATA							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
8	PDN CHA	PDN CHB	STDBY	DATA FORMAT	DIS CTRL PINS	TEST PAT ALIGN	0	RESET

Default: 00h

D[7:6]	**PDN CHA** and **PDN CHB**	Power-down channels A and B. Effective only when bit DIS CTRL PINS is set to '1'.
00	Normal operation	
01	Channel B powers down. Use only if the QDR interface is selected. Do not use in the DDR interface.	
10	Channel A powers down. Functions in both QDR and DDR interfaces.	
11	Both channels power down. Functions in both QDR and DDR interfaces.	
D5	**STDBY**	Dual ADC is placed into standby mode
0	Normal operation	
1	Power down	
D4	**DATA FORMAT**	Digital output data format
0	Twos complement	
1	Offset binary	
D3	**DIS CTRL PINS**	Disables power-down control from CTRL1, CTRL2 pins. This bit also functions as an enable bit for the INV CLK OUT CHA, INV CLK OUT CHB, and DDR OUTPUT TIMING bits.
0	CTRL1 and CTRL2 pins control power-down options for channels A and B	
1	Register bits PDN CHA and PDN CHB determine power-down options for channels A and B. Register bits INV CLK OUT CHA, INV CLK OUT CHB, and DDR OUTPUT TIMING become effective.	
D2	**TEST PAT ALIGN**	Aligns test patterns of two channels
0	Test patterns for channel A and channel B are free running	
1	Test patterns for both channels are synchronized	
D0	**RESET**	Software reset applied
	This bit resets all internal registers to the default values and self-clears to ‘0’	

REGISTER ADDRESS	REGISTER DATA							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
B	CHA GAIN					CHA GAIN EN	0	FLIP DATA

Default: 00h

D[7:3] **CHA GAIN** Digital gain for channel A. Effective when register bit CHA GAIN EN is set to '1'. Bit descriptions are listed in Table 9.

Table 9. Digital Gain for Channel A

DIGITAL GAIN FOR CHANNEL A	DIGITAL GAIN (dB)	MAX INPUT VOLTAGE (V_{PP})		DIGITAL GAIN FOR CHANNEL A	DIGITAL GAIN (dB)	MAX INPUT VOLTAGE (V_{PP})
00000	0	**2.0**		01010	1.5	1.7
00001	Do not use	—		01011	2	1.6
00010	Do not use	—		01100	2.5	1.5
00011	–2.0	**2.5**		01101	3	1.4
00100	–1.5	2.4		01110	3.5	1.3
00101	–1.0	2.2		01111	4	1.25
00110	–0.5	2.1		10000	4.5	1.2
00111	0	**2.0**		10001	5	1.1
01000	0.5	1.9		10010	5.5	1.05
01001	1	1.8		10011	6	1.0

D2 **CHA GAIN EN** Digital gain enable bit for channel A

0 Digital gain disabled

1 Digital gain enabled

D0 **FLIP DATA** Flips bit order on LVDS output bus (LSB versus MSB)

0 Normal operation

1 Output bus flipped. In the ADS42LB69, output data bit D0 becomes D15, D1 becomes D14, and so forth. In the ADS42LB49, output data bit D0 becomes D13, D1 becomes D12, and so forth.

REGISTER ADDRESS	REGISTER DATA							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
C	CHB GAIN					CHB GAIN EN	OVR ON LSB	

Default: 00h

D[7:3] **CHB GAIN** Digital gain for channel B. Effective when register bit CHB GAIN EN is set to '1'.Bit descriptions are listed in Table 10.

Table 10. Digital Gain for Channel B

DIGITAL GAIN FOR CHANNEL B	DIGITAL GAIN (dB)	MAX INPUT VOLTAGE (V_{PP})		DIGITAL GAIN FOR CHANNEL B	DIGITAL GAIN (dB)	MAX INPUT VOLTAGE (V_{PP})
00000	0	**2.0**		01010	1.5	1.7
00001	Do not use	—		01011	2	1.6
00010	Do not use	—		01100	2.5	1.5
00011	–2.0	**2.5**		01101	3	1.4
00100	–1.5	2.4		01110	3.5	1.3
00101	–1.0	2.2		01111	4	1.25
00110	–0.5	2.1		10000	4.5	1.2
00111	0	**2.0**		10001	5	1.1
01000	0.5	1.9		10010	5.5	1.05
01001	1	1.8		10011	6	1.0

D2 **CHB GAIN EN** Digital gain enable bit for channel B

0 Digital gain disabled

1 Digital gain disabled

D[1:0] **OVR ON LSB** Functions only with the DDR interface option. Replaces the LSB pair of 16-bit data (D1, D0) with OVR information. See the *Overrange Indication* section.

00 D1 and D0 are output in the ADS42LB69, NC for the ADS42LB49

01 Fast OVR in LVDS logic level

10 Normal OVR in LVDS logic level

11 D1 and D0 are output in the ADS42LB69, NC for the ADS42LB49

REGISTER ADDRESS	REGISTER DATA							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
D	0	1	1	0	1	1	0	FAST OVR ON PIN

Default: 6Ch

D0 **FAST OVR ON PIN** Determines whether normal OVR or fast OVR information is brought on the OVRx, CTRL1, and CTRL2 pins. See the *Overrange Indication* section.

0 Normal OVR available on the OVRx, CTRL1, and CTRL2 pins

1 Fast OVR available on the OVRx, CTRL1, and CTRL2 pins

REGISTER ADDRESS	REGISTER DATA							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
F	CHA TEST PATTERNS				CHB TEST PATTERNS			

Default: 00h

D[7:4]	**CHA TEST PATTERNS**	Channel A test pattern programmability
0000	Normal Operation	
0001	Outputs all 0s	
0010	Outputs all 1s	
0011	Outputs toggle pattern:	In the ADS42LB69, data are an alternating sequence of *1010101010101010* and *0101010101010101*. In the ADS42LB49, data alternate between *10101010101010* and *01010101010101*.
0100	Output digital ramp:	In the ADS42LB69, data increment by 1 LSB every clock cycle from code 0 to 65535. In the ADS42LB49 data increment by 1 LSB every fourth clock cycle from code 0 to 16383.
0101	Increment pattern:	Do not use
0110	Single pattern:	In the ADS42LB69, data are the same as programmed by registers bits CUSTOM PATTERN 1[15:0]. In the ADS42LB49, data are the same as programmed by register bits CUSTOM PATTERN 1[15:2].
0111	Double pattern:	In the ADS42LB69, data alternate between CUSTOM PATTERN 1[15:0] and CUSTOM PATTERN 2[15:0]. In the ADS42LB49 data alternate between CUSTOM PATTERN 1[15:2] and CUSTOM PATTERN 2[15:2].
1000	Deskew pattern:	In the ADS42LB69, data are AAAAh. In the ADS42LB49, data are 3AAAh.
1001	Do not use	
1010	PRBS pattern:	Data are a sequence of pseudo-random numbers
1011	8P sine:	In the ADS42LB69, data are a repetitive sequence of the following eight numbers, forming a sine-wave in twos complement format: 1, 9598, 32768, 55938, 65535, 55938, 32768, and 9598. In the ADS42LB49, data are a repetitive sequence of the following eight numbers, forming a sine-wave in twos complement format: 0, 2399, 8192, 13984, 16383, 13984, 8192, and 2399.
D[3:0]	**CHB TEST PATTERNS**	Channel B test pattern programmability
0000	Normal Operation	
0001	Outputs all 0s	
0010	Outputs all 1s	
0011	Outputs toggle pattern:	In the ADS42LB69, data are an alternating sequence of *1010101010101010* and *0101010101010101*. In the ADS42LB49, data alternate between *10101010101010* and *01010101010101*.
0100	Output digital ramp:	In the ADS42LB69, data increment by 1 LSB every clock cycle from code 0 to 65535. In the ADS42LB49 data increment by 1 LSB every fourth clock cycle from code 0 to 16383.
0101	Increment pattern:	Do not use
0110	Single pattern:	In the ADS42LB69, data are the same as programmed by registers bits CUSTOM PATTERN 1[15:0]. In the ADS42LB49, data are the same as programmed by register bits CUSTOM PATTERN 1[15:2].
0111	Double pattern:	In the ADS42LB69, data alternate between CUSTOM PATTERN 1[15:0] and CUSTOM PATTERN 2[15:0]. In the ADS42LB49 data alternate between CUSTOM PATTERN 1[15:2] and CUSTOM PATTERN 2[15:2].
1000	Deskew pattern:	In the ADS42LB69, data are AAAAh. In the ADS42LB49, data are 3AAAh.
1001	Do not use	
1010	PRBS pattern:	Data are a sequence of pseudo-random numbers
1011	8P sine:	In the ADS42LB69, data are a repetitive sequence of the following eight numbers, forming a sine-wave in twos complement format: 1, 9598, 32768, 55938, 65535, 55938, 32768, and 9598. In the ADS42LB49, data are a repetitive sequence of the following eight numbers, forming a sine-wave in twos complement format: 0, 2399, 8192, 13984, 16383, 13984, 8192, and 2399.

REGISTER ADDRESS	REGISTER DATA							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
10	CUSTOM PATTERN 1 (15:8)							

Default: 00h

D[7:0] **CUSTOM PATTERN 1 (15:8)** Sets the custom pattern 1[15:8] with these bits for both channels

REGISTER ADDRESS	REGISTER DATA							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
11	CUSTOM PATTERN 1 (7:0)							

Default: 00h

D[7:0] **CUSTOM PATTERN 1 (7:0)** Sets the custom pattern 1[7:0] with these bits for both channels

REGISTER ADDRESS	REGISTER DATA							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
12	CUSTOM PATTERN 2 (15:8)							

Default: 00h

D[7:0] **CUSTOM PATTERN 2 (15:8)** Sets the custom pattern 2[15:8] with these bits for both channels

REGISTER ADDRESS	REGISTER DATA							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
13	CUSTOM PATTERN 2 (7:0)							

Default: 00h

D[7:0] **CUSTOM PATTERN 2 (7:0)** Sets the custom pattern 2[7:0] with these bits for both channels

REGISTER ADDRESS	REGISTER DATA							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
14	0	0	0	0	LVDS CLK STRENGTH	LVDS DATA STRENGTH	DISABLE OUTPUT CHA	DISABLE OUTPUT CHB

Default: 00h

D3 **LVDS CLK STRENGTH** Increases the LVDS drive strength of the CLKOUTP, CLKOUTM buffers in the DDR pinout and the DxCLKP, DxCLKM buffers in the QDR pinout

0 LVDS output clock buffer at default strength used with 100-Ω external termination

1 LVDS output clock buffer has double strength used with 50-Ω external termination. Effective only when bit LVDS CLK STRENGTH EN is set to '1'.

D2 **LVDS DATA STRENGTH** Increases the LVDS drive strength

0 LVDS output data buffers (including frame clock buffers in the QDR interface) at default strength used with a 100-Ω external termination

1 LVDS output data buffers (including frame clock buffers in the QDR interface) at double strength used with a 50-Ω external termination

D1 **DISABLE OUTPUT CHA** Disables LVDS output buffers of channel A

0 Normal operation

1 Channel A output buffers are in 3-state

D0 **DISABLE OUTPUT CHB** Disables LVDS output buffers of channel B

0 Normal operation

1 Channel B output buffers are in 3-state

REGISTER ADDRESS	REGISTER DATA							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
15	0	0	0	0	0	0	0	DDR - QDR

Default: 00h

D0 **DDR – QDR** Selects output interface between DDR and QDR LVDS mode

0 QDR LVDS mode

1 DDR LVDS mode

REGISTER ADDRESS	REGISTER DATA							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
16	0	0	DDR OUTPUT TIMING					0

Default: 00h

D[5:1] **DDR OUTPUT TIMING** Effective only when bit DIS CTRL PINS is set to '1'. Bit descriptions are listed in Table 11.

Table 11. DDR Output Timing (After Setting bits DIS CTRL PINS to '1')

BIT SETTING	DELAY (ps) IN OUTPUT CLOCK WITH RESPECT TO DEFAULT POSITION			
	f_S = 250 MSPS	f_S = 200 MSPS	f_S = 150 MSPS	f_S = 100 MSPS
00101	–180	–220	–310	–440
00111	–100	–130	–190	–260
00000	0	0	0	0
01101	120	130	170	260
01110	230	240	330	520
01011	320	360	480	740
10100	400	460	620	940
10000	500	600	790	1220

Register Address	Register Data							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
17	LVDS CLK STRENGTH EN	0	QDR OUTPUT TIMING CHA					INVCLK OUT CHA

Default: 00h

D7 **LVDS CLK STRENGTH EN**

0 Default

1 Enables clock strength programmability with LVDS CLK STRENGTH bit

D[5:1] **QDR OUTPUT TIMING CHA** Adjusts position of output data clock on chA with respect to output data. Bit settings are listed in Table 12.

D0 **INV CLK OUT CHA** Inverts polarity of the output clock for channel A (QDR mode only)

0 Normal operation

1 Polarity of channel A output clock DACLKP, DACLKM is inverted. Effective only when bit DIS CTRL PINS is set to '1'.

Table 12. QDR Timing Channel A Timing

BIT SETTING	DELAY (ps) IN OUTPUT CLOCK WITH RESPECT TO DEFAULT POSITION			
	f_S = 250 MSPS	f_S = 200 MSPS	f_S = 150 MSPS	f_S = 100 MSPS
00101	–80	–120	–150	–225
00111	–55	–75	–90	–130
00000	0	0	0	0
01101	55	65	90	130
01110	95	115	165	235
01011	140	165	230	350
10100	180	220	290	450
10000	230	290	370	565

REGISTER ADDRESS	REGISTER DATA							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
18	0	0	QDR OUTPUT TIMING CHB					INVCLK OUT CHB

Default: 00h

D[5:1] **QDR OUTPUT TIMING CHB** Adjusts position of output data clock on chB with respect to output data. Bit settings are listed in Table 13.

D0 **INV CLK OUT CHB** Inverts output clock polarity for channel B in QDR mode, or output clock CLKOUTP, CLKOUTM in DDR mode.

0 Normal operation

1 In QDR mode, the polarity of the channel B output clock DBCLKP, DBCLKM is inverted. Effective only when bit DIS CTRL PINS is set to '1'. In DDR mode, the output clock polarity of CLKOUTP, CLKOUTM is inverted.

Table 13. QDR Timing Channel B Timing

BIT SETTING	DELAY (ps) IN OUTPUT CLOCK WITH RESPECT TO DEFAULT POSITION			
	f_S = 250 MSPS	f_S = 200 MSPS	f_S = 150 MSPS	f_S = 100 MSPS
00101	–80	–120	–150	–225
00111	–55	–75	–90	–130
00000	0	0	0	0
01101	55	65	90	130
01110	95	115	165	235
01011	140	165	230	350
10100	180	220	290	450
10000	230	290	370	565

REGISTER ADDRESS	REGISTER DATA							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
1F	Always write '0'	FAST OVR THRESHOLD						

Default: FFh

D7 **Always write '0'**

Default value of this bit is '1'. Always write this bit to '0' when fast OVR thresholds are programmed.

D[6:0] **FAST OVR THRESHOLD**

The device has a fast OVR mode that indicates an overload condition at the ADC input. The input voltage level at which the overload is detected is referred to as the threshold and is programmable using the FAST OVR THRESHOLD bits. FAST OVR is triggered nine output clock cycles after the overload condition occurs. The threshold at which fast OVR is triggered is (full-scale × [the decimal value of the FAST OVR THRESHOLD bits] / 127). See the *Overrange Indication* section for details.

REGISTER ADDRESS	REGISTER DATA							
A7-A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
20	0	0	0	0	0	0	0	PDN/OVR FOR CTRL PINS

Default: 00h

D0 **PDN/OVR FOR CTRL PINS** Determines if the CTRL1, CTRL2 pins are power-down control or OVR outputs

0 CTRL1 and CTRL2 pins function as input pins to control power-down operation.

1 CTRL1 and CTRL2 pins function as output pins for overrange indications of channels A and B, respectively. Register bits PDN CH A, PDN CH B along with DIS CTRL PINS can be used for power-down operation.

APPLICATION INFORMATION

THEORY OF OPERATION

The ADS42LB69 and ADS42LB49 is a family of high linearity, buffered analog input, dual-channel ADCs with maximum sampling rates up to 250 MSPS employing either a quadruple data rate (QDR) or double data rate (DDR) LVDS interface. The conversion process is initiated by a rising edge of the external input clock and the analog input signal is sampled. The sampled signal is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline, resulting in a data latency of 14 clock cycles. The output is available in LVDS logic levels in SPI-programmable QDR or DDR options.

ANALOG INPUT

The analog input pins have analog buffers (running from the AVDD3V supply) that internally drive the differential sampling circuit. As a result of the analog buffer, the input pins present high input impedance to the external driving source (at dc, a 10-kΩ differential input resistance is provided in shunt with a 4-pF differential input capacitance). The buffer helps isolate the external driving source from the switching currents of the sampling circuit. This buffering makes driving the buffered inputs easier than when compared to an ADC without the buffer.

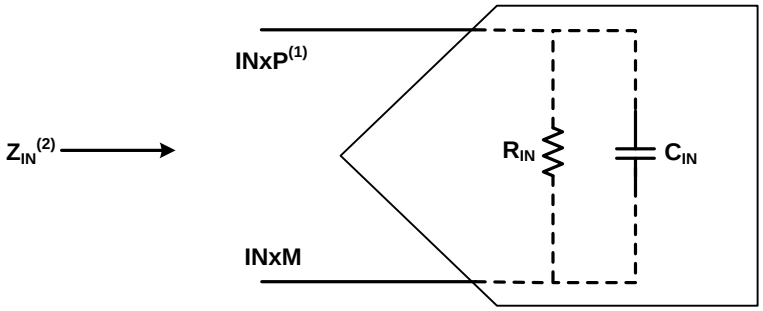
The input common-mode is set internally using a 5-kΩ resistor from each input pin to VCM so the input signal can be ac-coupled to the pins. Each input pin (INP, INM) must swing symmetrically between VCM + 0.5 V and VCM – 0.5 V, resulting in a 2-V_{PP} differential input swing. When programmed for 2.5-V_{PP} full-scale, each input pin must swing symmetrically between VCM + 0.625 V and VCM – 0.625 V.

The input sampling circuit has a high 3-dB bandwidth that extends up to 900 MHz (measured with a 50-Ω source driving a 50-Ω termination between INP and INM). The dynamic offset of the first-stage sub-ADC limits the maximum analog input frequency to approximately 250 MHz (with a 2.5-V_{PP} full-scale amplitude) and to approximately 400 MHz (with a 2-V_{PP} full-scale amplitude). This maximum analog input frequency is different than the analog bandwidth of 900 MHz, which is only an indicator of signal amplitude versus frequency.

Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This technique improves the common-mode noise immunity and even-order harmonic rejection. A small resistor (10 Ω) in series with each input pin is recommended to damp out ringing caused by package parasitics.

Figure 85, Figure 86, and Figure 87 show the differential impedance ($Z_{IN} = R_{IN} \parallel C_{IN}$) at the ADC input pins. The presence of the analog input buffer results in an almost constant input capacitance up to 1 GHz.



(1) X = A or B.

(2) $Z_{IN} = R_{IN} \parallel (1 / j\omega C_{IN})$.

Figure 85. ADC Equivalent Input Impedance

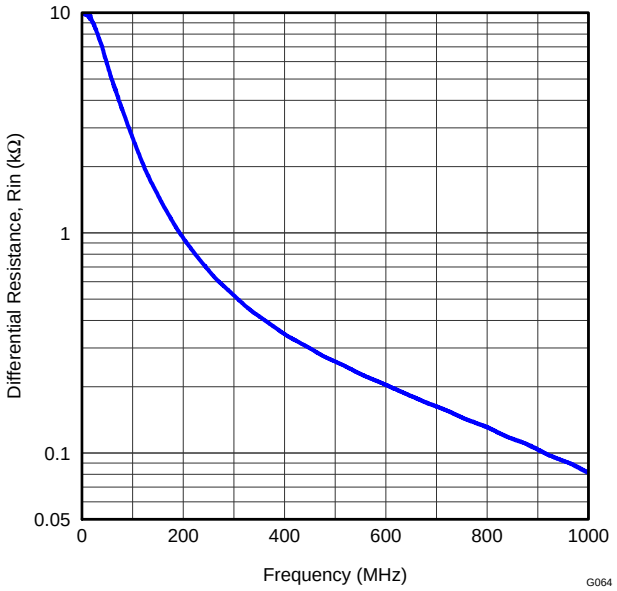


Figure 86. ADC Analog Input Resistance (R_{IN}) Across Frequency

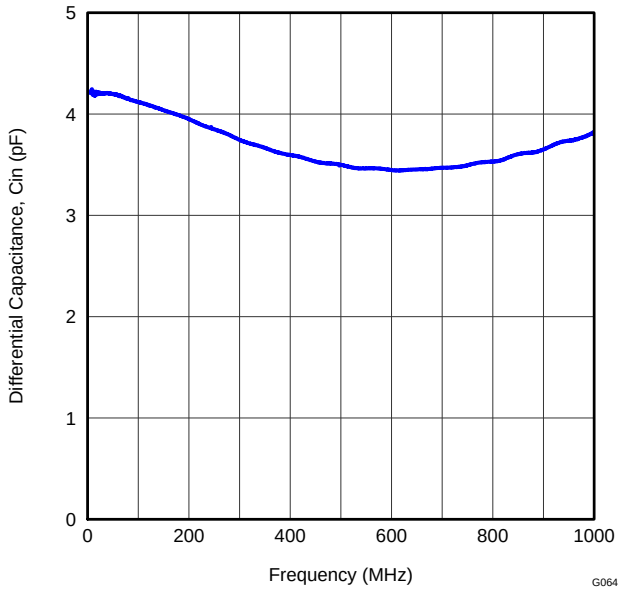


Figure 87. ADC Analog Input Capacitance (C_{IN}) Across Frequency

Driving Circuit

An example driving circuit configuration is shown in Figure 88. To optimize even-harmonic performance at high input frequencies (greater than the first Nyquist), the use of back-to-back transformers is recommended, as shown in Figure 88. Note that the drive circuit is terminated by 50 Ω near the ADC side. The ac-coupling capacitors allow the analog inputs to self-bias around the required common-mode voltage. If HD2 optimization is a concern, using a 10-Ω series resistor on the INP side and a 9.5-Ω series resistor on the INM side may help improve HD2 by 2 dB to 3 dB at a 85-dBFS level on a 170-MHz IF. An additional R-C-R (39 Ω - 6.8 pF - 39 Ω) circuit placed near device pins helps further improve HD3.

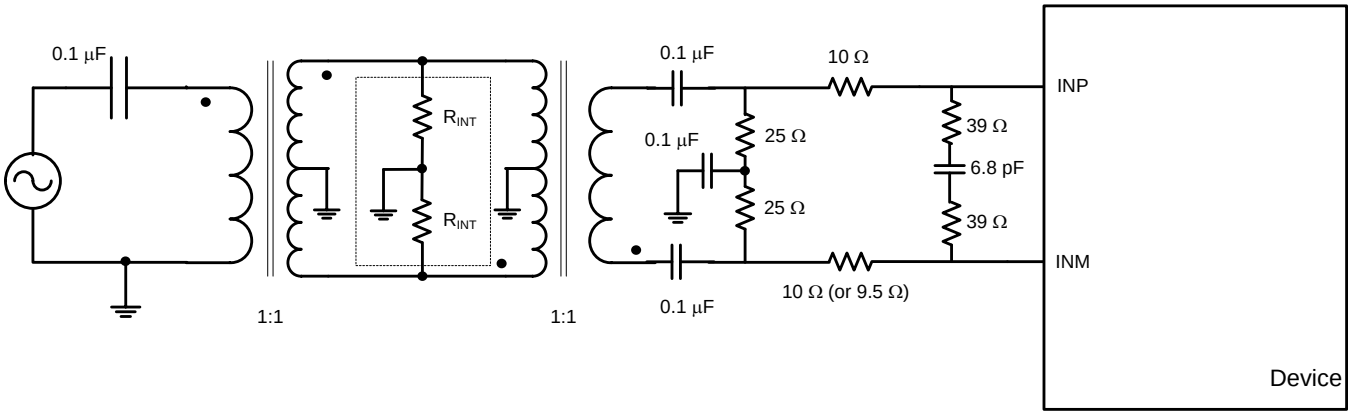


Figure 88. Drive Circuit for Input Frequencies Up to 250 MHz

The mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch and good performance is obtained for high-frequency input signals. An additional termination resistor pair may be required between the two transformers, as shown in Figure 88. The center point of this termination is connected to ground to improve the balance between the P (positive) and M (negative) sides. The values of the terminations between the transformers and on the secondary side must be chosen to obtain an effective 50 Ω (for a 50-Ω source impedance). For high input frequencies (>250MHz), the R-C-R circuit can be removed as indicated in Figure 89.

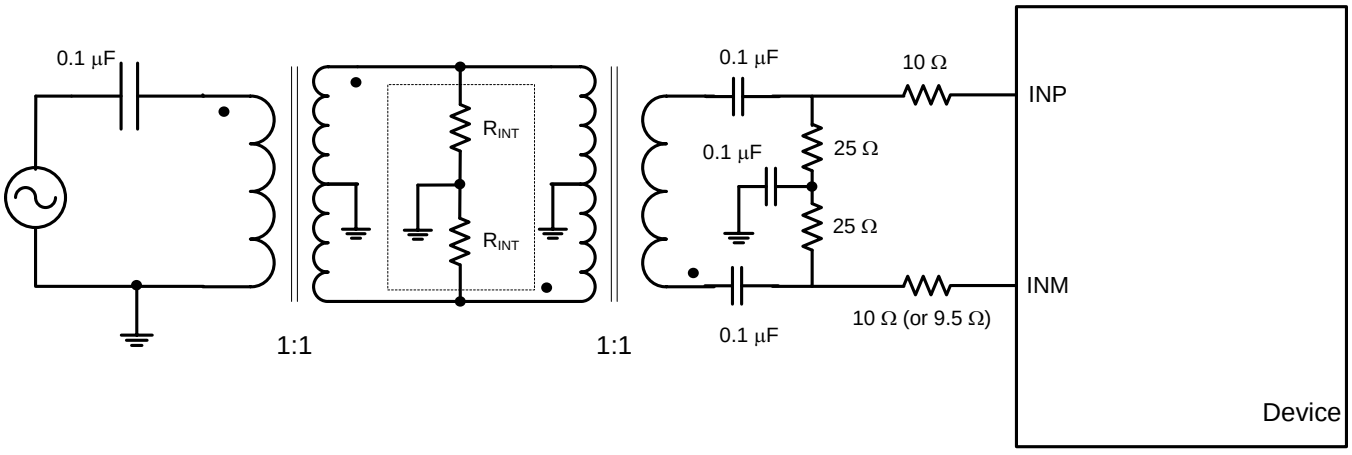
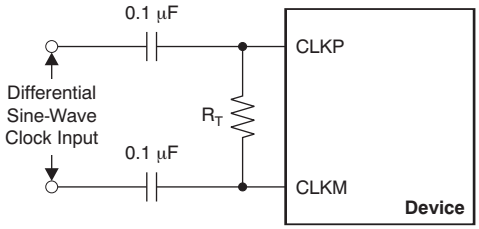


Figure 89. Drive Circuit for Input Frequencies > 250 MHz

CLOCK INPUT

The device clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to 1.4 V using internal 5-kΩ resistors. The self-bias clock inputs of the ADS42LB69 and ADS42LB49 can be driven by the transformer-coupled, sine-wave clock source or by the ac-coupled, LVPECL and LVDS clock sources, as shown in Figure 90, Figure 91, and Figure 92. See Figure 92 for details regarding the internal clock buffer.



NOTE: R_T = termination resistor, if necessary.

Figure 90. Differential Sine-Wave Clock Driving Circuit

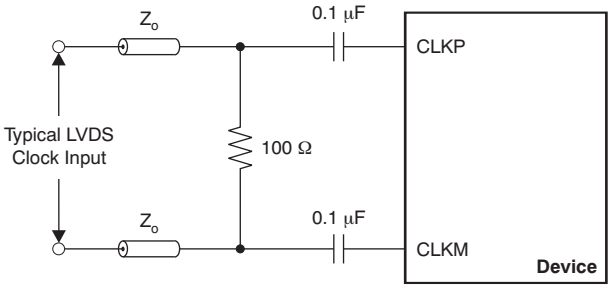


Figure 91. LVDS Clock Driving Circuit

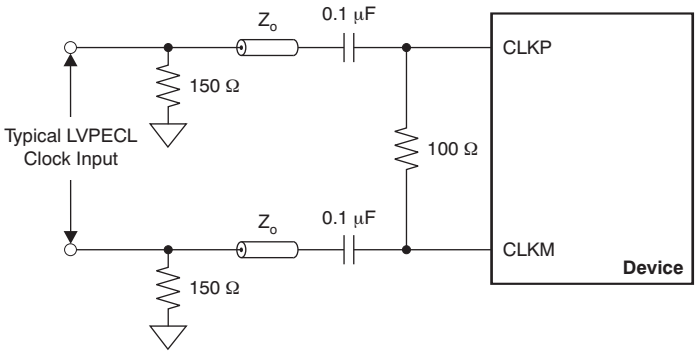
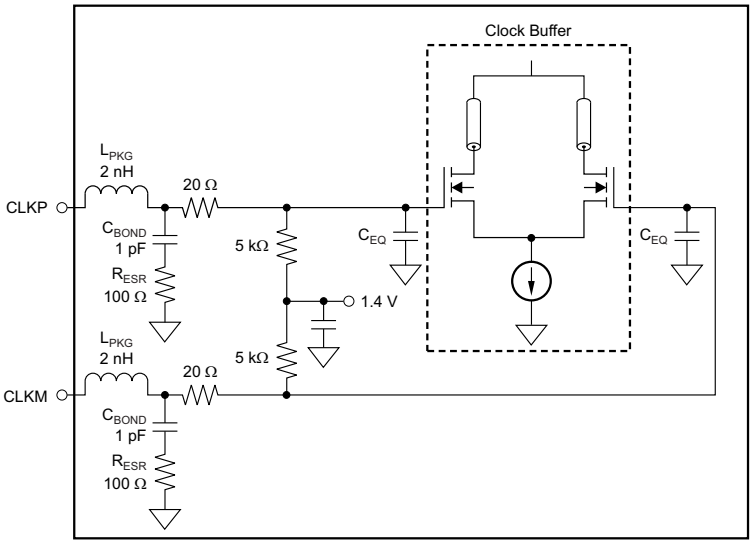


Figure 92. LVPECL Clock Driving Circuit



NOTE: C_{EQ} is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

Figure 93. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-µF capacitor, as shown in Figure 94. However, for best performance the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, TI recommends using a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

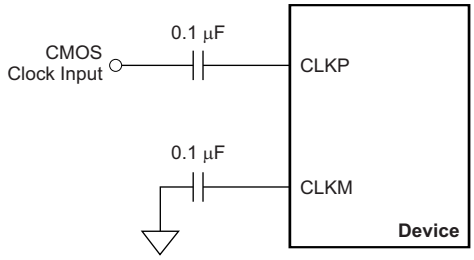


Figure 94. Single-Ended Clock Driving Circuit

DIGITAL GAIN

The device includes gain settings that can be used to obtain improved SFDR performance (compared to no gain). Gain is programmable from –2 dB to 6 dB (in 0.5-dB steps). For each gain setting, the analog input full-scale range scales proportionally. Table 14 shows how full-scale input voltage changes when digital gain are programmed in 1-dB steps. Refer to Table 9 to set digital gain using a serial interface register.

SFDR improvement is achieved at the expense of SNR; for a 1-dB increase in digital gain, SNR degrades approximately between 0.5 dB and 1 dB (refer to Figure 25 and Figure 26). Therefore, gain can be used as a trade-off between SFDR and SNR. Note that the default gain after reset is 0 dB with a 2.0-V_{PP} full-scale voltage.

Table 14. Full-Scale Range Across Gains

DIGITAL GAIN	FULL-SCALE INPUT VOLTAGE
–2 dB	2.5 V_{PP} (1)
–1 dB	2.2 V_{PP}
0 dB (default)	2.0 V_{PP}
1 dB	1.8 V_{PP}
2 dB	1.6 V_{PP}
3 dB	1.4 V_{PP}
4 dB	1.25 V_{PP}
5 dB	1.1 V_{PP}
6 dB	1.0 V_{PP}

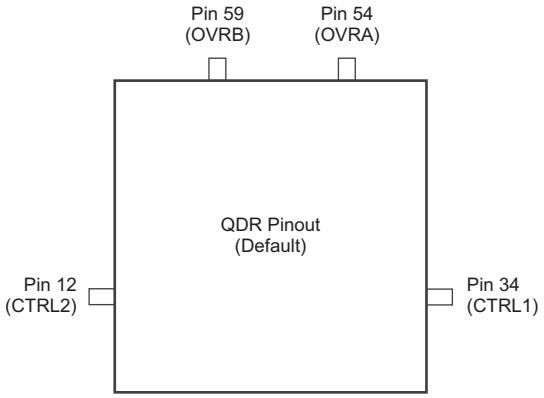
(1) Shaded cells indicate performance settings used in the Electrical Characteristics and Typical Characteristics.

OVERRANGE INDICATION

The device provides two different overrange indications: normal OVR and fast OVR. Normal OVR (default) is triggered if the final 16-bit data output exceeds the maximum code value. Normal OVR latency is the same as the output data (that is, 14 clock cycles). Fast OVR is triggered if the input voltage exceeds the programmable overrange threshold and is presented after a latency of only nine clock cycles, thus enabling a quicker reaction to an overrange event.

OVR In a QDR Pinout

In a QDR interface, the overrange indication is output on the OVRA and OVRB pins (pin 54 and 59) in 1.8-V CMOS logic levels. The same overrange indication can also be made available on the bidirectional CTRL1, CTRL2 pins by using the PDN/OVR FOR CTRL PINS register bit, as described in Figure 95. Using the FAST OVR EN register bit, the fast OVR indication can be presented on these pins instead of normal OVR.



NOTE: By default, normal OVR is output on the OVRA and OVRB pins. Using the FAST OVR EN register bit, fast OVR can be presented on these pins instead.

NOTE: When the PDN/OVR FOR CTRL PINS register bit is set, the CTRL1 and CTRL2 pins function as output pins and carry the same information as the OVRA and OVRB pins (respectively) in 1.8-V CMOS logic levels.

Figure 95. OVR In a QDR Pinout

OVR In a DDR Pinout

In the DDR interface, there are no dedicated pins to provide overrange indication. However, by choosing the appropriate register bits, OVR can be transferred on the LSB of 16-bit output data as well as on the bidirectional CTRL1 and CTRL2 pins, as shown in Figure 96.

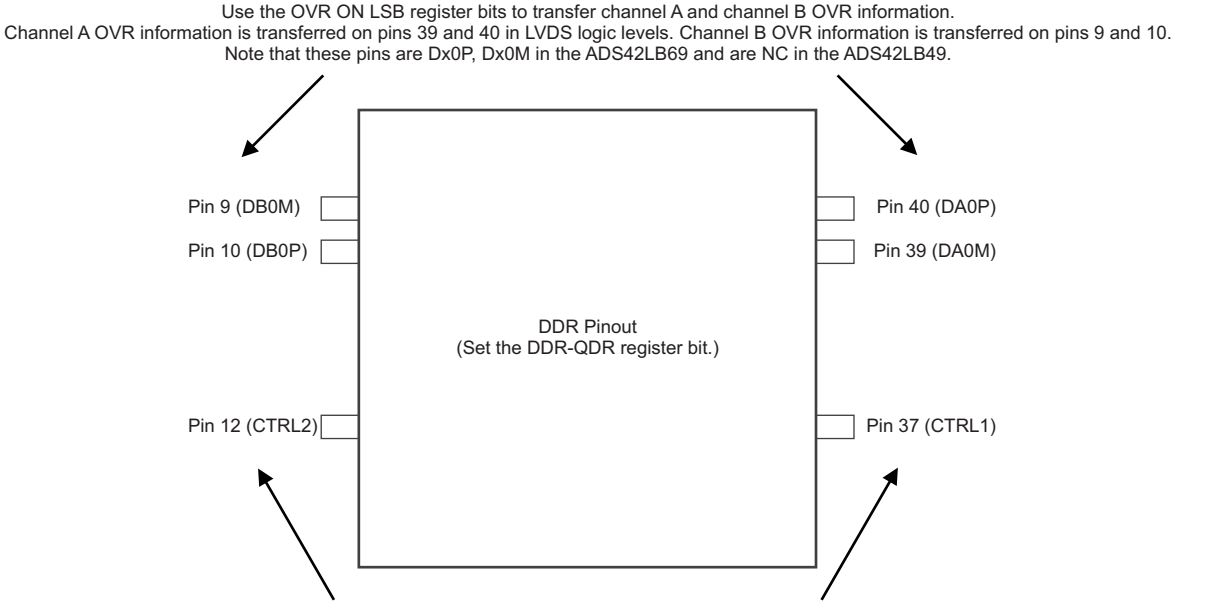


Figure 96. OVR In a DDR Pinout

The FAST OVR EN register bit can be used to transfer fast OVR indication on the CTRL1 and CTRL2 pins instead of normal OVR. The OVR ON LSB register bits can be used to transfer fast OVR indication on the LSB bits (Dx0P, Dx0M), as described in Table 15.

Table 15. Fast OVR Transfer

OVR ON LSB BIT SETTINGS	PIN STATE FOR PINS 9, 10 AND 39, 40
00	D0 and D1 are output in the ADS42LB69, NC for the ADS42LB49
01	Fast OVR in LVDS logic level
10	Normal OVR in LVDS logic level
11	D0 and D1 are output in the ADS42LB69, NC for the ADS42LB49

Table 16 summarizes the availability of OVR information on different pins in the QDR and DDR interfaces and the required register settings.

Table 16. OVR Information Availability

INTERFACE	SETTINGS	OVR INFORMATION AVAILABILITY		
		PINS 9, 10 AND 39, 40 (LVDS Logic Levels)	PINS 12 AND 37 (CMOS Logic Levels)	PINS 54 AND 59 (CMOS Logic Levels)
QDR	Default	Not applicable	No	Yes
	Use the PDN/OVR FOR CTRL PINS register bits	Not applicable	Yes	Yes
DDR	Default	No	No	Not applicable
	Use the OVR ON LSB register bits	Yes	No	Not applicable
	Use the PDN/OVR FOR CTRL PINS register bits	No	Yes	Not applicable
	Use the OVR ON LSB and PDN/OVR FOR CTRL PINS register bits	Yes	Yes	Not applicable

Programming Threshold for Fast OVR

The input voltage level at which the overload is detected is referred to as the threshold and is programmable using the FAST OVR THRESHOLD bits. Fast OVR is triggered nine output clock cycles after the overload condition occurs. The threshold voltage amplitude at which fast OVR is triggered is Equation 1:

1 × [the decimal value of the FAST OVR THRESH bits] / 127 (1)

When digital gain is programmed (for gain values > 0 dB), the threshold voltage amplitude is Equation 2:

$10^{-\text{ Gain / 20}}$ x [the decimal value of the FAST OVR THRESH bits] / 127 (2)

SNR AND CLOCK JITTER

The signal-to-noise ratio (SNR) of the ADC is limited by three different factors, as shown in Equation 3. Quantization noise is typically not noticeable in pipeline converters and is 96 dBFS for a 16-bit ADC. Thermal noise limits SNR at low input frequencies and clock jitter sets SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20 \times \log \sqrt{\left(10 - \frac{SNR_{Quantization\_Noise}}{20}\right)^2 + \left(10 - \frac{SNR_{ThermalNoise}}{20}\right)^2 + \left(10 - \frac{SNR_{Jitter}}{20}\right)^2} \quad (3)$$

SNR limitation is a result of sample clock jitter and can be calculated by Equation 4:

$$SNR_{Jitter}\ [dBc] = -20 \times \log(2\pi \times f_{IN} \times t_{Jitter}) \quad (4)$$

The total clock jitter (T_{Jitter}) has three components: the internal aperture jitter (85 f_S for the device) is set by the noise of the clock input buffer, the external clock jitter, and the jitter from the analog input signal. T_{Jitter} can be calculated by Equation 5:

$$T_{Jitter} = \sqrt{(T_{Jitter,Ext.Clock\_Input})^2 + (T_{Aperture\_ADC})^2} \quad (5)$$

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input while a faster clock slew rate improves ADC aperture jitter. The device has a 74.1-dBFS thermal noise and an 85-f_S internal aperture jitter. The SNR value depends on the amount of external jitter for different input frequencies, as shown in Figure 97.

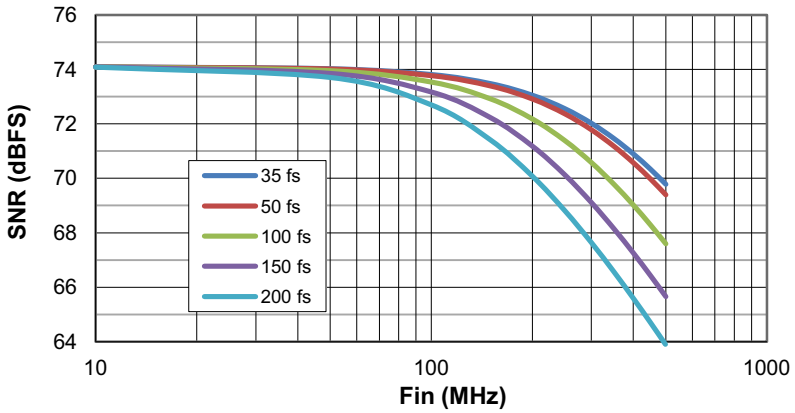


Figure 97. SNR versus Input Frequency and External Clock Jitter

INPUT CLOCK DIVIDER

The device is equipped with an internal divider on the clock input. This divider allows operation with a faster input clock, simplifying the system clock distribution design. The clock divider can be bypassed (divide-by-1) for operation with a 250-MHz clock. The divide-by-2 option supports a maximum 500-MHz input clock and the divide-by-4 option supports a maximum 1-GHz input clock frequency.

DIGITAL OUTPUT INFORMATION

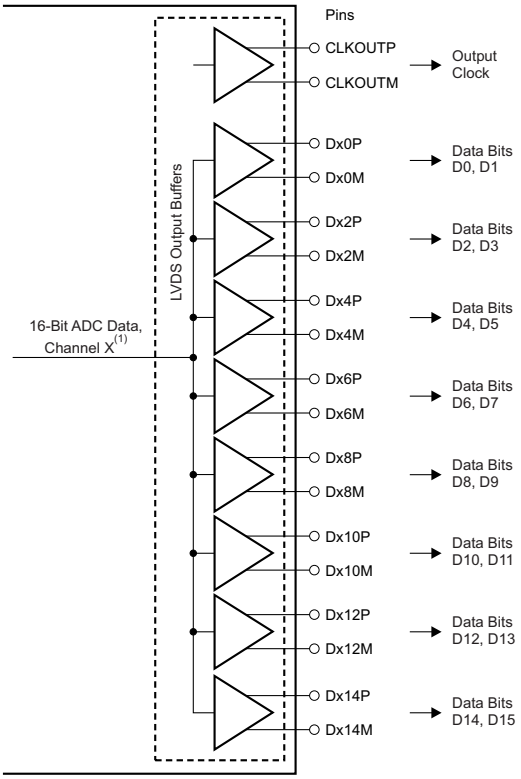
The ADS42LB49 and ADS42LB69 provides 14- and 16-bit digital data for each channel and output clock synchronized with the data.

Output Interface

Digital outputs are available in quadruple data rate (QDR) LVDS, and double data rate (DDR) LVDS formats, selectable by the DDR - QDR serial register bit.

DDR LVDS Outputs

In this mode, the data bits and clock are output using low-voltage differential signal (LVDS) levels. Two data bits are multiplexed and output on each LVDS differential pair, as shown in Figure 98.



(1) X = A or B (for channel A or channel B).

Figure 98. DDR LVDS Interface

Even data bits (D0, D2, D4, and so forth) are output at the CLKOUTP rising edge and the odd data bits (D1, D3, D5, and so forth) are output at the CLKOUTP falling edge. Both the CLKOUTP rising and falling edges must be used to capture all the data bits, as shown in Figure 99.

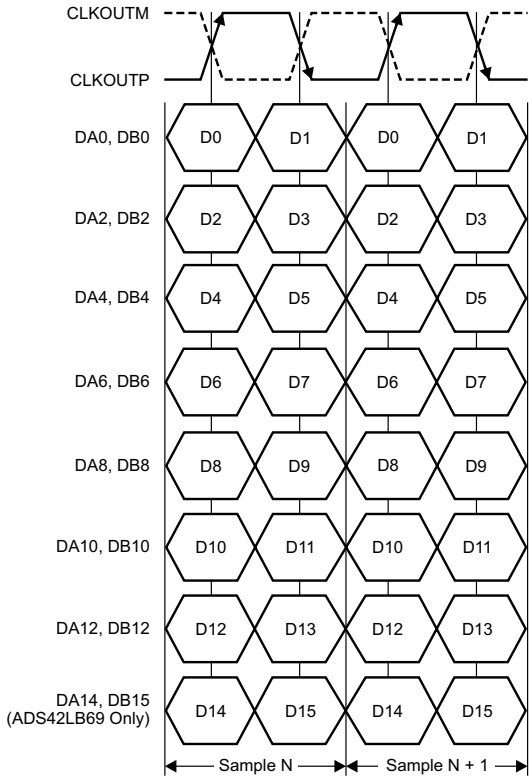
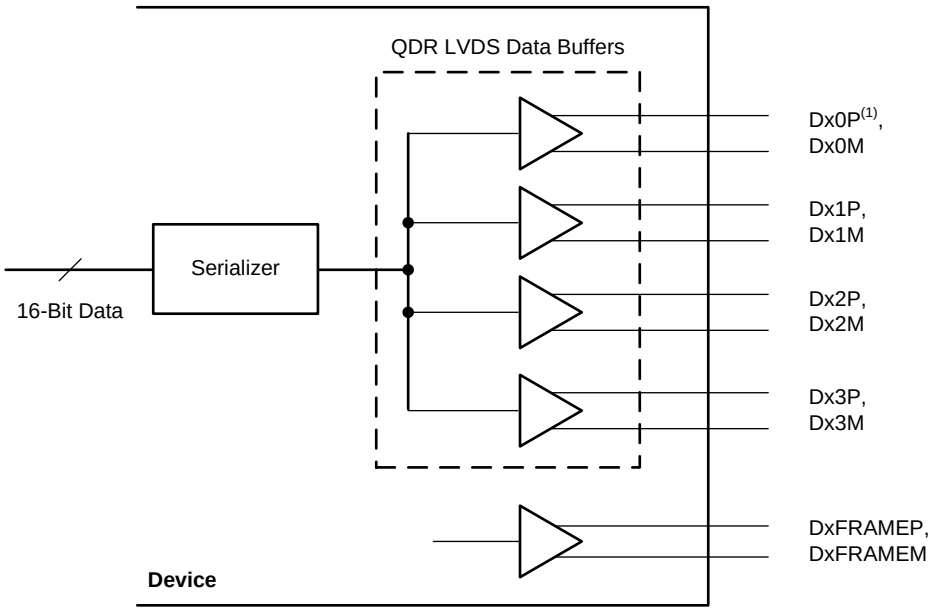


Figure 99. DDR LVDS Interface Timing

QDR LVDS Outputs

The data bits and output clocks are output using low-voltage differential signal (LVDS) levels. Four data bits are multiplexed and output on each LVDS differential data pair and are accompanied by a bit clock and a frame clock for each channel, as shown in Figure 100.



(1) X = channels A and B.

Figure 100. QDR LVDS Interface

Figure 101 shows the QDR interface bit order for the ADS42LB69 and Figure 102 shows the QDR interface bit order for the ADS42LB49.

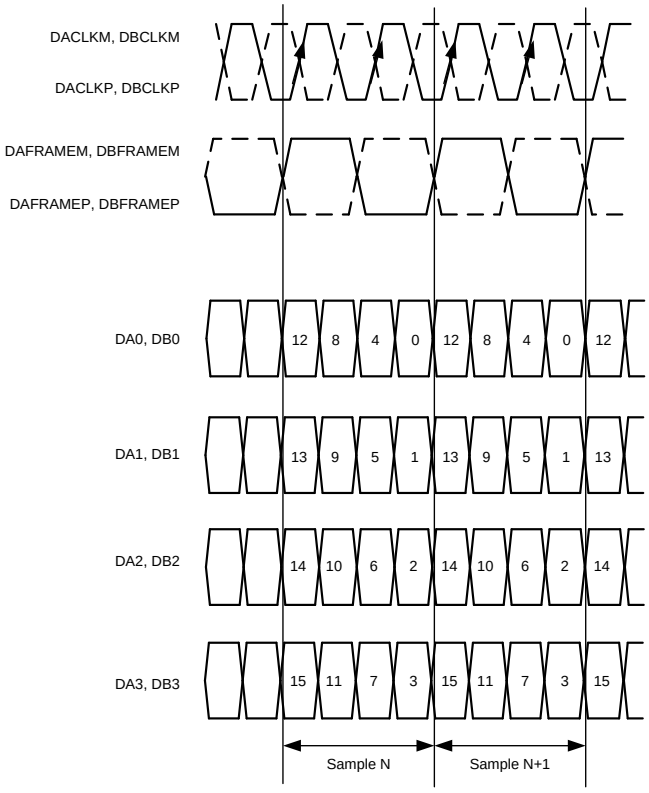


Figure 101. QDR LVDS Interface Timing: ADS42LB69

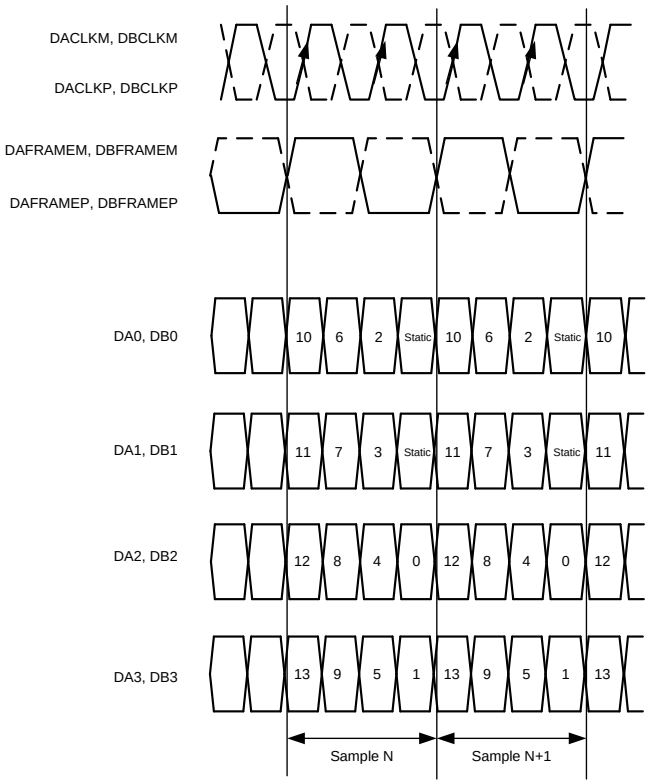
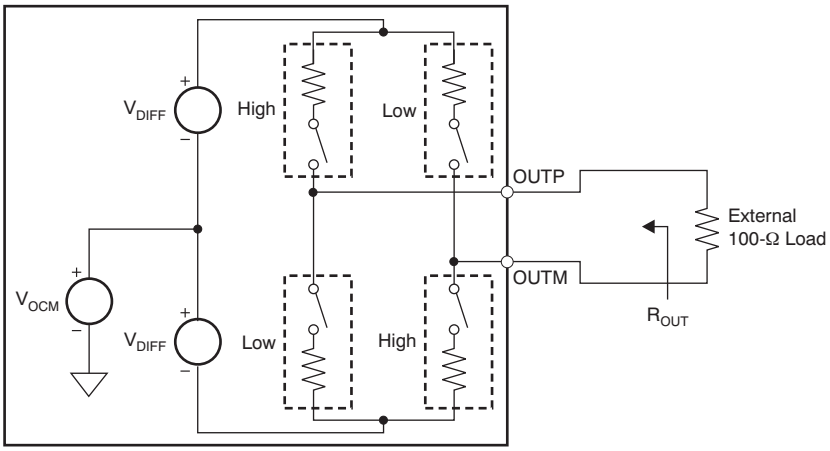


Figure 102. QDR LVDS Interface Timing: ADS42LB49

LVDS Buffer

The equivalent circuit of each LVDS output buffer is shown in Figure 103. After reset, the buffer presents an output impedance of 100 Ω to match with the external 100-Ω termination.



NOTE: Default swing across 100-Ω load is ±350 mV. Use the LVDS SWING bits to change the swing.

Figure 103. LVDS Buffer Equivalent Circuit

The V_{DIFF} voltage is nominally 350 mV, resulting in an output swing of ±350 mV with 100-Ω external termination. The V_{DIFF} voltage is programmable using the LVDS SWING register bits from ±125 mV to ±570 mV.

Additionally, a mode exists to double the strength of the LVDS buffer to support 50-Ω differential termination, as shown in Figure 104. This mode can be used when the output LVDS signal is routed to two separate receiver chips, each using a 100-Ω termination. The mode can be enabled for LVDS output data (and for the frame clock in the QDR interface) buffers by setting the LVDS DATA STRENGTH register bit. For LVDS output clock buffers (applicable for both DDR and QDR interfaces), set both the LVDS CLKOUT STRENGTH EN and LVDS CLKOUT STRENGTH register bits to '1'.

The buffer output impedance behaves in the same way as a source-side series termination. Absorbing reflections from the receiver end helps improve signal integrity.

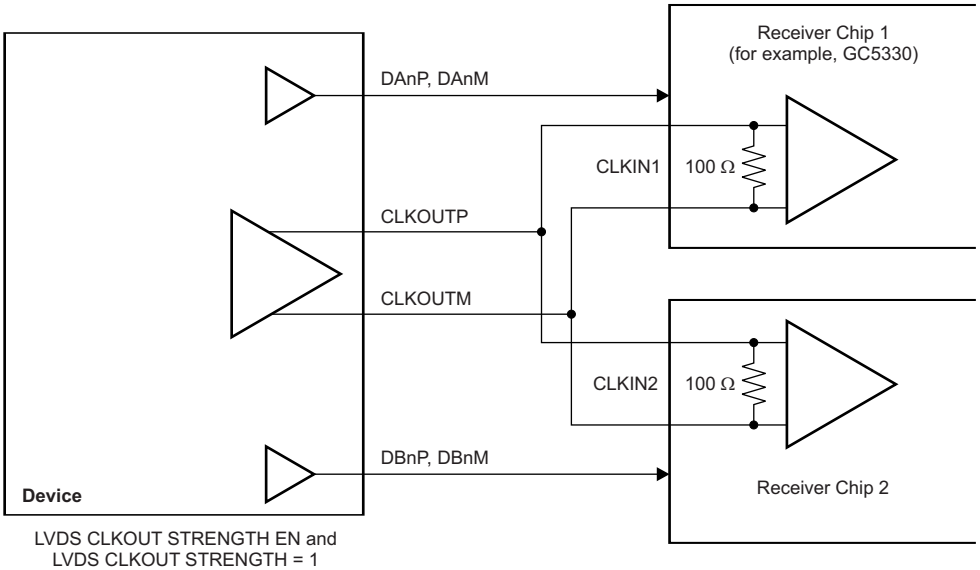


Figure 104. LVDS Buffer Differential Termination

Output Data Format

Two output data formats are supported: twos complement and offset binary. The format can be selected using the DATA FORMAT serial interface register bit.

In the event of an input voltage overdrive, the digital outputs go to the appropriate full-scale level. For a positive overdrive, the output code is 3FFFh for the ADS42LB49 and ADS42LB69 in offset binary output format; the output code is 1FFFh for the ADS42LB49 and ADS42LB69 in twos complement output format. For a negative input overdrive, the output code is 0000h in offset binary output format and 2000h for the ADS42LB49 and ADS42LB69 in twos complement output format.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (September 2013) to Revision D **Page**

- Changed device status to Production Data 1
- Added pre-RTM changes throughout document 1

Changes from Revision B (March 2013) to Revision C **Page**

- Added pre-RTM changes throughout document 1

Changes from Revision A (November 2012) to Revision B **Page**

- Added pre-RTM changes throughout document 1

Changes from Original (October 2012) to Revision A **Page**

- Added pre-RTM changes throughout document 1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS42LB49IRGC25	ACTIVE	VQFN	RGC	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AZ42LB49	Samples
ADS42LB49IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AZ42LB49	Samples
ADS42LB49IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AZ42LB49	Samples
ADS42LB69IRGC25	ACTIVE	VQFN	RGC	64	25	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AZ42LB69	Samples
ADS42LB69IRGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AZ42LB69	Samples
ADS42LB69IRGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU | Call TI	Level-3-260C-168 HR	-40 to 85	AZ42LB69	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

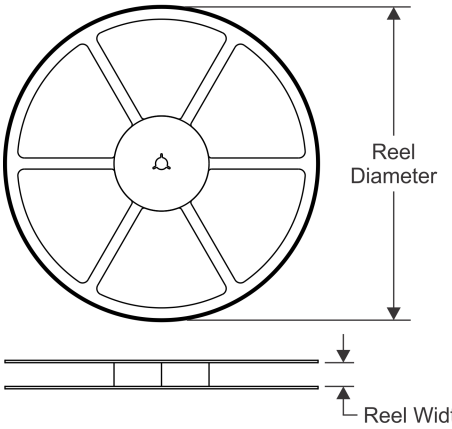
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

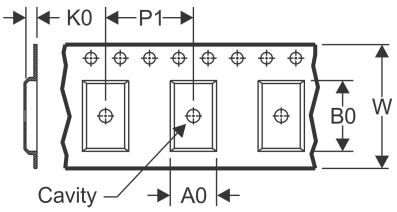
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

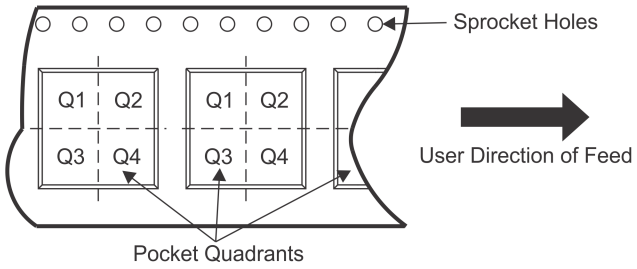


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

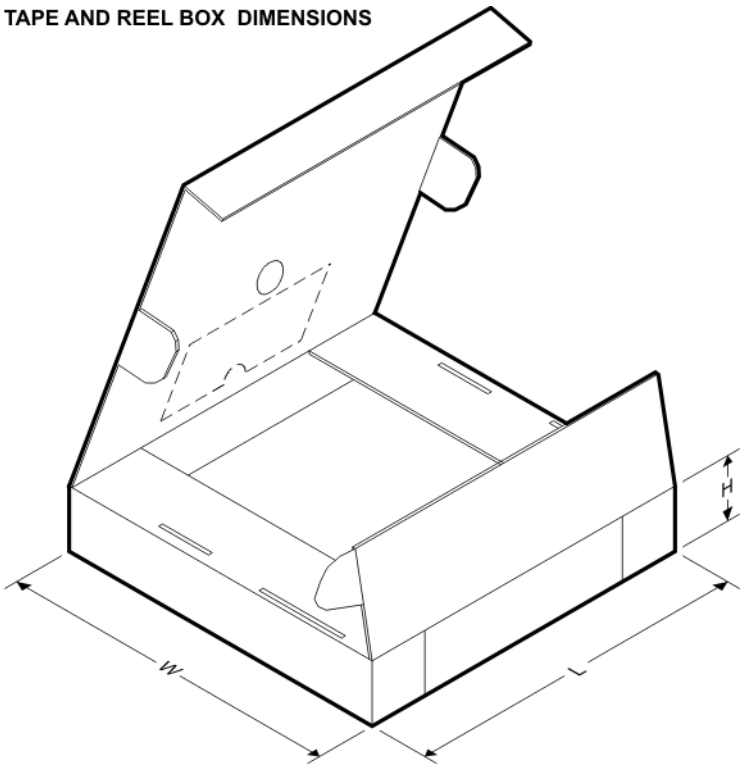
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS42LB49IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS42LB49IRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS42LB69IRGCR	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
ADS42LB69IRGCT	VQFN	RGC	64	250	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

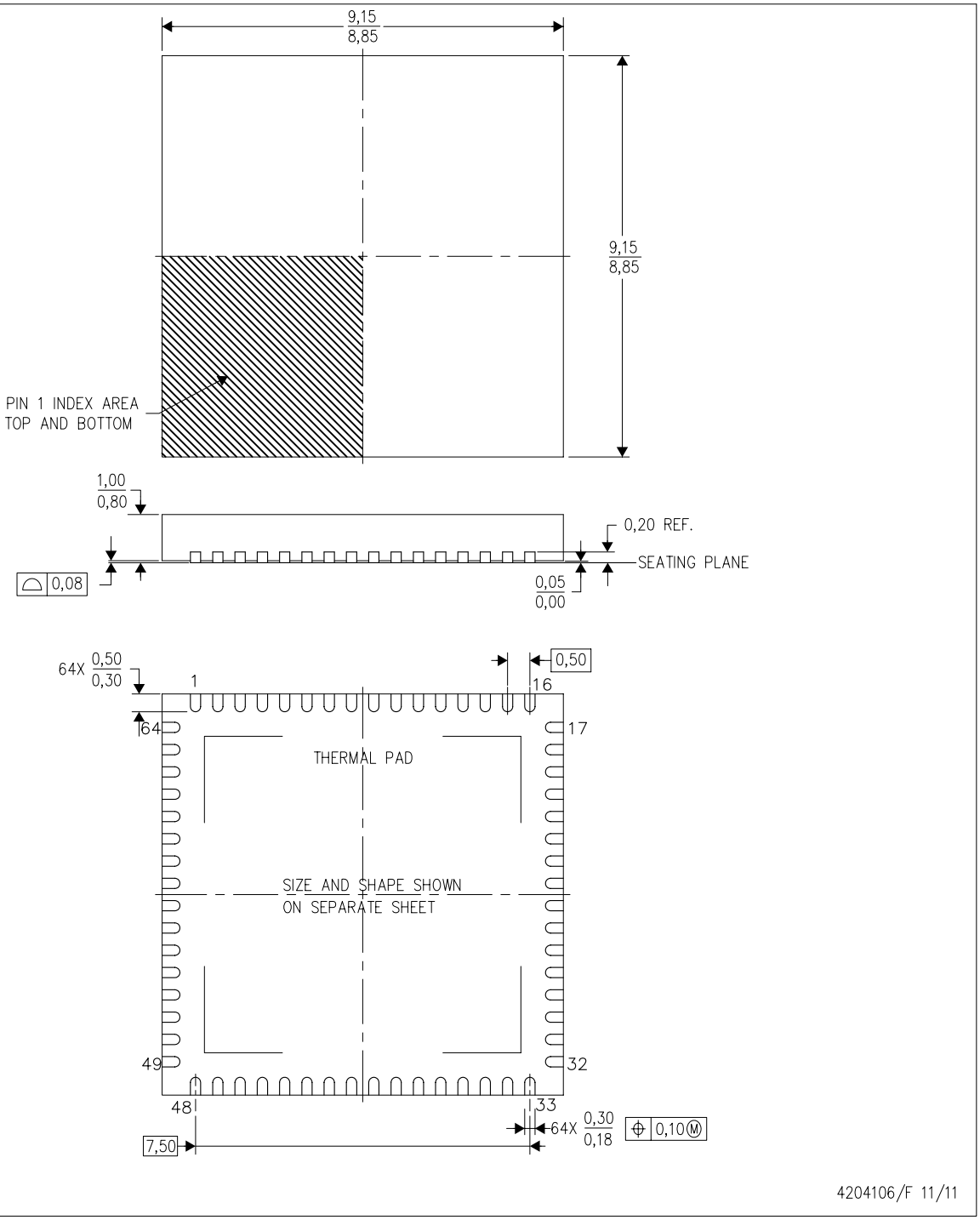
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS42LB49IRGCR	VQFN	RGC	64	2000	336.6	336.6	28.6
ADS42LB49IRGCT	VQFN	RGC	64	250	336.6	336.6	28.6
ADS42LB69IRGCR	VQFN	RGC	64	2000	336.6	336.6	28.6
ADS42LB69IRGCT	VQFN	RGC	64	250	336.6	336.6	28.6

RGC(S–PVQFN–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

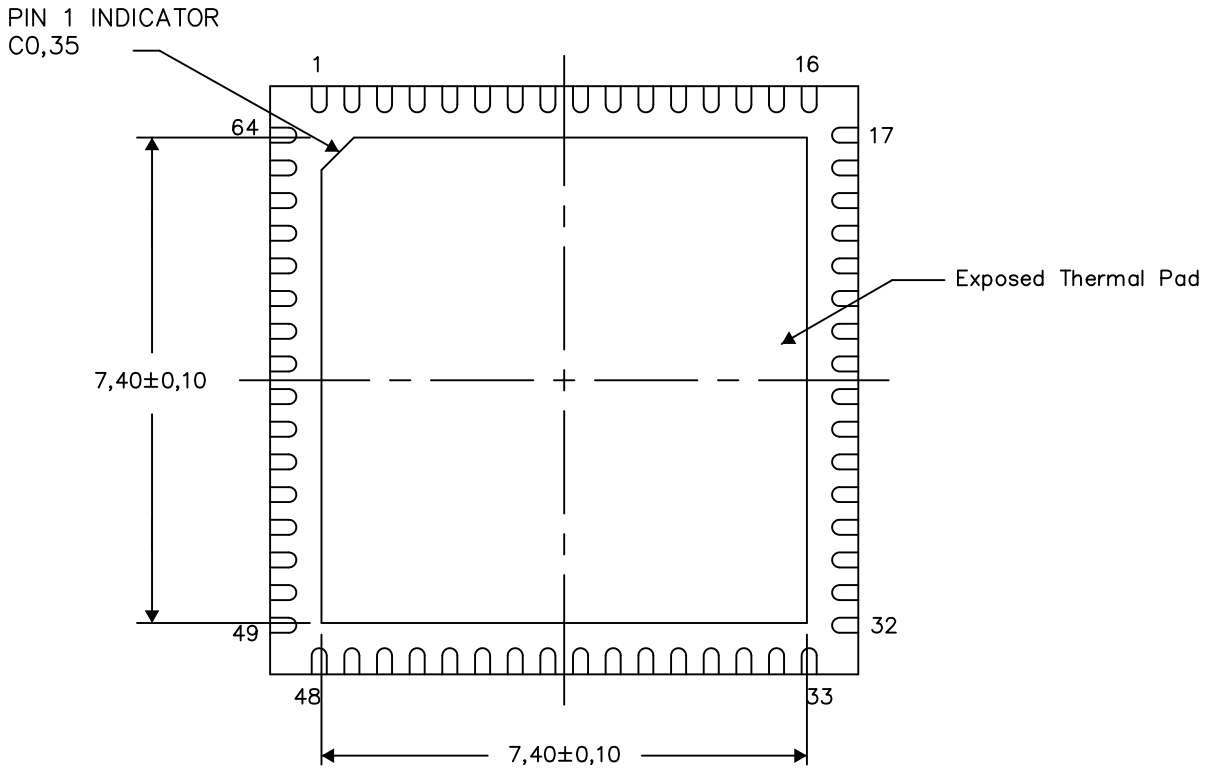
RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



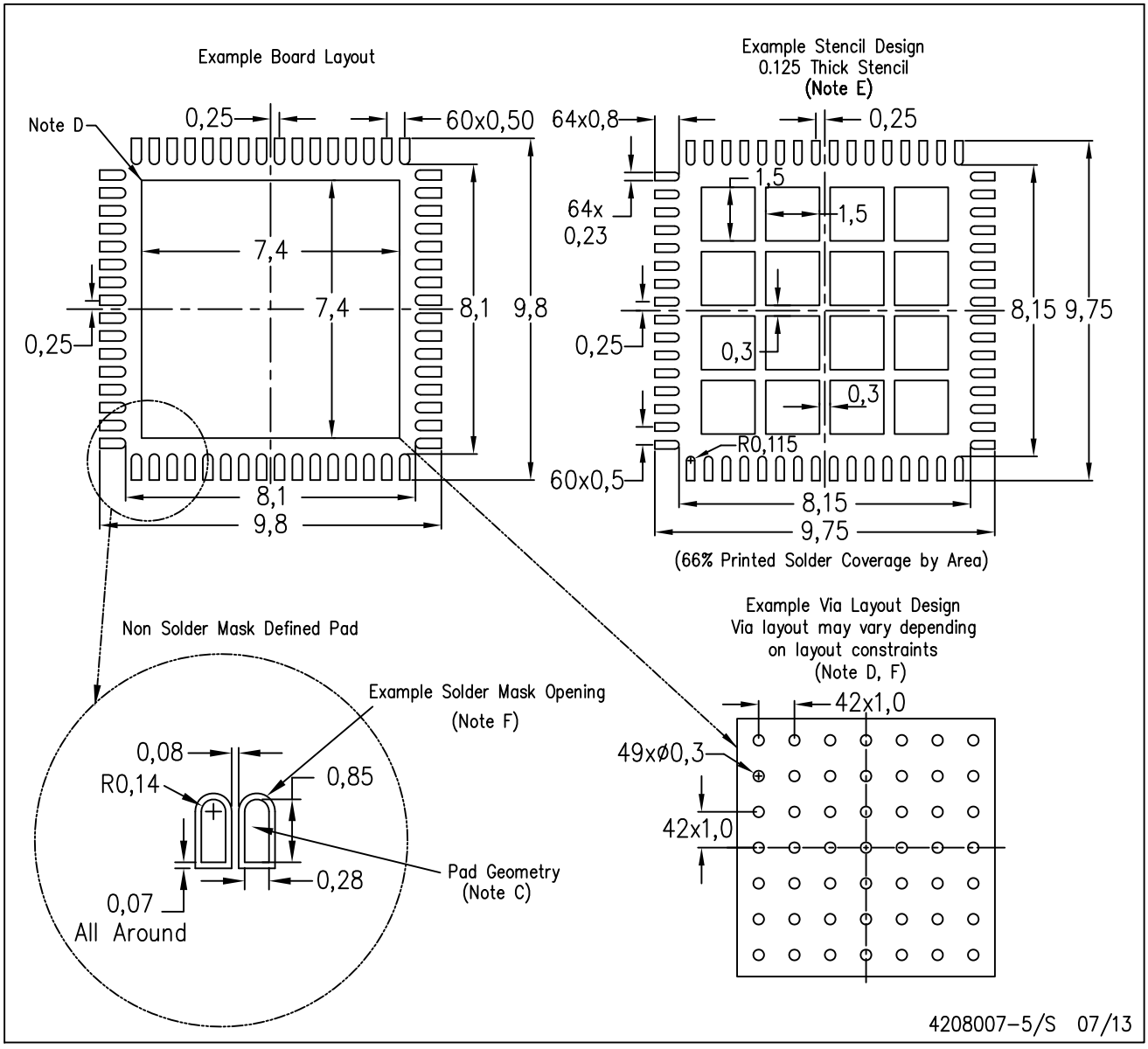
Bottom View

Exposed Thermal Pad Dimensions

4206192–4/AB 10/13

NOTE: A. All linear dimensions are in millimeters

RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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